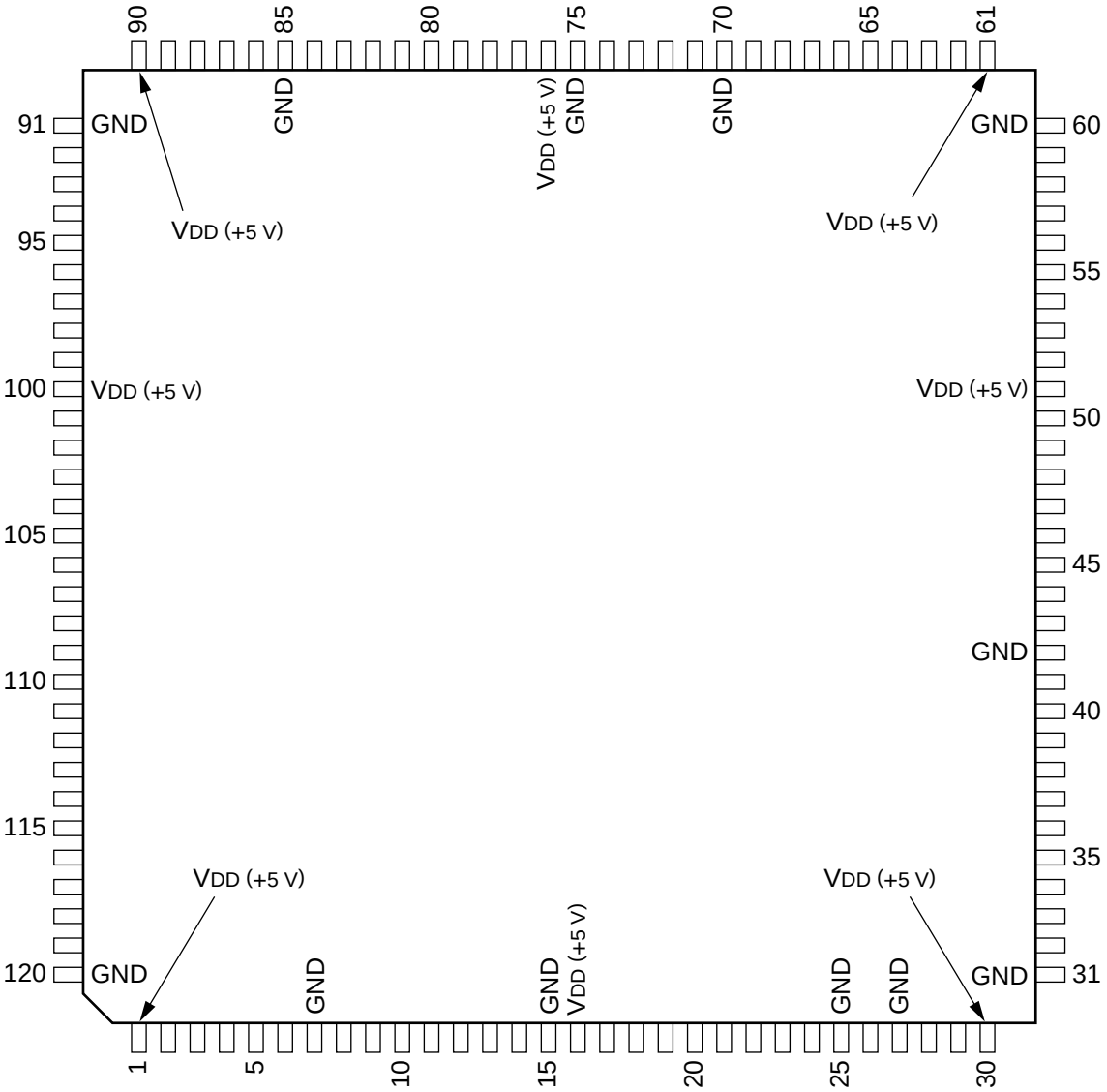
C-MOS GATE ARRAY

—TOP VIEW—



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	V_{DD}	31	—	GND	61	—	V_{DD}	91	—	GND
2	I	XCS0	32	O	RAM XHWE	62	I/O	DR8	92	I/O	D7
3	I	XCS1	33	O	RAM XLWE	63	I/O	DR9	93	I/O	D6
4	I	CS2	34	O	RAM XOE	64	I/O	DR10	94	I/O	D5
5	I	CS3	35	O	AR14	65	I/O	DR11	95	I/O	D4
6	I	CS4	36	O	AR13	66	I/O	DR12	96	I/O	D3
7	—	GND	37	O	AR12	67	I/O	DR13	97	I/O	D2
8	I	ST	38	O	AR11	68	I/O	DR14	98	I/O	D1
9	I	DIN11	39	O	AR10	69	I/O	DR15	99	I/O	D0
10	I	DIN10	40	O	AR9	70	—	GND	100	—	V_{DD}
11	I	DIN9	41	O	AR8	71	O	DOUT0	101	I	A0
12	I	DIN8	42	—	GND	72	O	DOUT1	102	I	A1
13	I	DIN7	43	O	AR7	73	O	DOUT2	103	I	A2
14	I	DIN6	44	O	AR6	74	O	DOUT3	104	I	A3
15	—	GND	45	O	AR5	75	—	GND	105	I	A4
16	—	V_{DD}	46	O	AR4	76	—	V_{DD}	106	I	A5
17	I	DIN5	47	O	AR3	77	O	DOUT4	107	I	A6
18	I	DIN4	48	O	AR2	78	O	DOUT5	108	I	A7
19	I	DIN3	49	O	AR1	79	O	DOUT6	109	I	A8
20	I	DIN2	50	O	AR0	80	O	DOUT7	110	I	A9
21	I	DIN1	51	—	V_{DD}	81	O	DOUT8	111	I	A10
22	I	DIN0	52	I/O	DR0	82	O	DOUT9	112	I	A11
23	I	DCK	53	I/O	DR1	83	O	DOUT10	113	I	A12
24	I	XDRES	54	I/O	DR2	84	O	DOUT11	114	I	A13
25	—	GND	55	I/O	DR3	85	—	GND	115	I	A14
26	I	SYSCK	56	I/O	DR4	86	O	XHVALID	116	I	A15
27	—	GND	57	I/O	DR5	87	O	XVVALID	117	I	A16
28	I	XRST	58	I/O	DR6	88	I	COL0	118	I	XRD
29	I	TEST	59	I/O	DR7	89	I	COL1	119	I	XWR
30	—	V_{DD}	60	—	GND	90	—	V_{DD}	120	—	GND