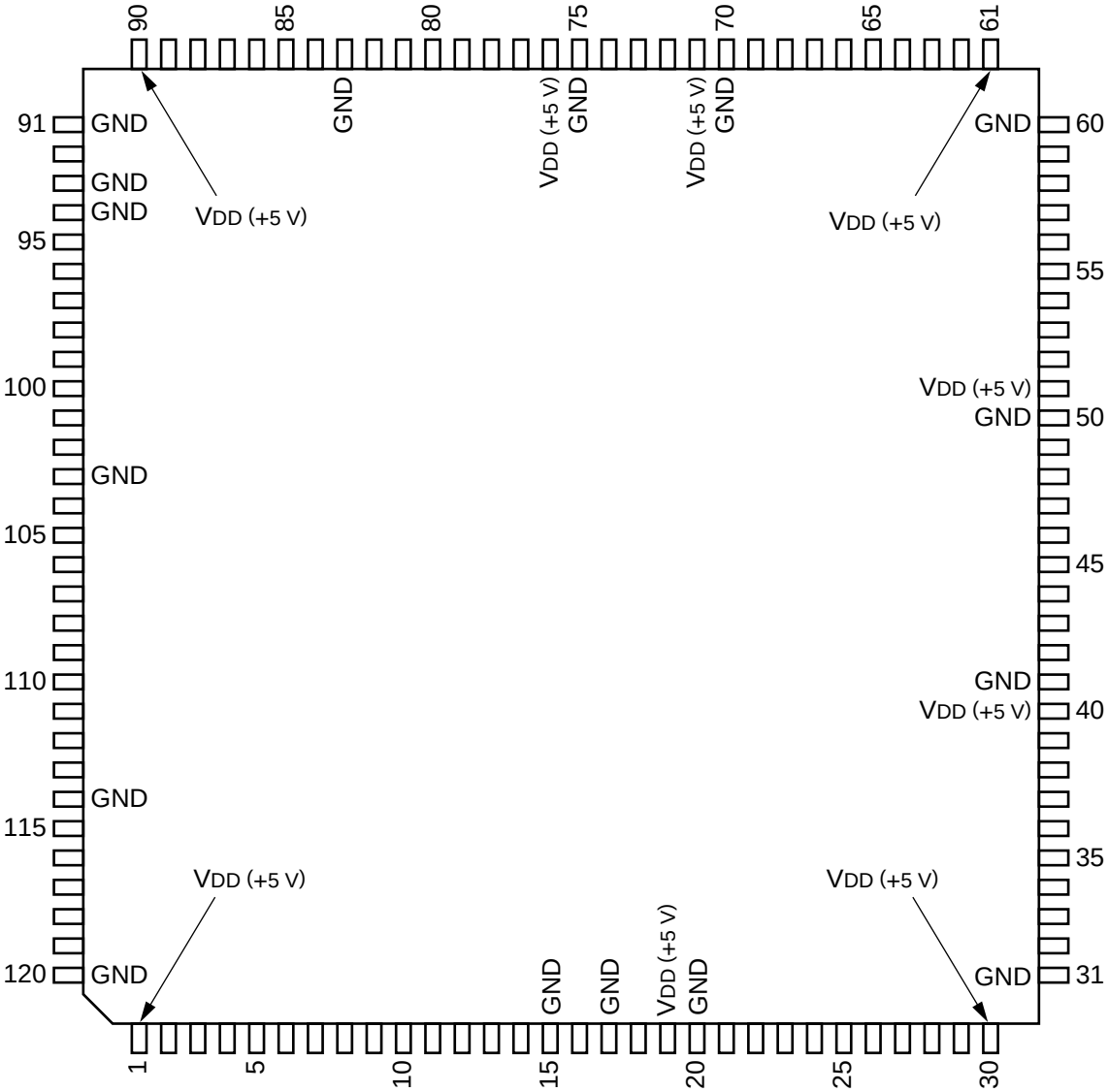
C-MOS GATE ARRAY

—TOP VIEW—



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	V_{DD}	31	—	GND	61	—	V_{DD}	91	—	GND
2	I	DIN11	32	O	AR7	62	I/O	DR16	92	O	XDVALID
3	I	DIN10	33	O	AR6	63	I/O	DR17	93	—	GND
4	I	DIN9	34	O	AR5	64	I/O	DR18	94	—	GND
5	I	DIN8	35	O	AR4	65	I/O	DR19	95	I	D7
6	I	DIN7	36	O	AR3	66	I/O	DR20	96	I	D6
7	I	DIN6	37	O	AR2	67	I/O	DR21	97	I	D5
8	I	DIN5	38	O	AR1	68	I/O	DR22	98	I	D4
9	I	DIN4	39	O	AR0	69	I/O	DR23	99	I	D3
10	I	DIN3	40	—	V_{DD}	70	—	GND	100	I	D2
11	I	DIN2	41	—	GND	71	—	V_{DD}	101	I	D1
12	I	DIN1	42	I/O	DR0	72	—	NC	102	I	D0
13	I	DIN0	43	I/O	DR1	73	—	NC	103	—	GND
14	I	DCK	44	I/O	DR2	74	—	NC	104	I	A0
15	—	GND	45	I/O	DR3	75	—	GND	105	I	A1
16	I	SYSCK	46	I/O	DR4	76	—	V_{DD}	106	I	A2
17	—	GND	47	I/O	DR5	77	O	DOUT0	107	I	A3
18	I	XRST	48	I/O	DR6	78	O	DOUT1	108	I	A4
19	—	V_{DD}	49	I/O	DR7	79	O	DOUT2	109	I	XWR
20	—	GND	50	—	GND	80	O	DOUT3	110	I	XCS0
21	O	XWE	51	—	V_{DD}	81	O	DOUT4	111	I	XCS1
22	O	XOE	52	I/O	DR8	82	O	DOUT5	112	I	CS2
23	O	AR14	53	I/O	DR9	83	—	GND	113	I	CS3
24	O	AR13	54	I/O	DR10	84	O	DOUT6	114	—	GND
25	O	AR12	55	I/O	DR11	85	O	DOUT7	115	I	TEST
26	O	AR11	56	I/O	DR12	86	O	DOUT8	116	I	COL1
27	O	AR10	57	I/O	DR13	87	O	DOUT9	117	I	COL0
28	O	AR9	58	I/O	DR14	88	O	DOUT10	118	I	XVVALID
29	O	AR8	59	I/O	DR15	89	O	DOUT11	119	I	XHVALID
30	—	V_{DD}	60	—	GND	90	—	V_{DD}	120	—	GND