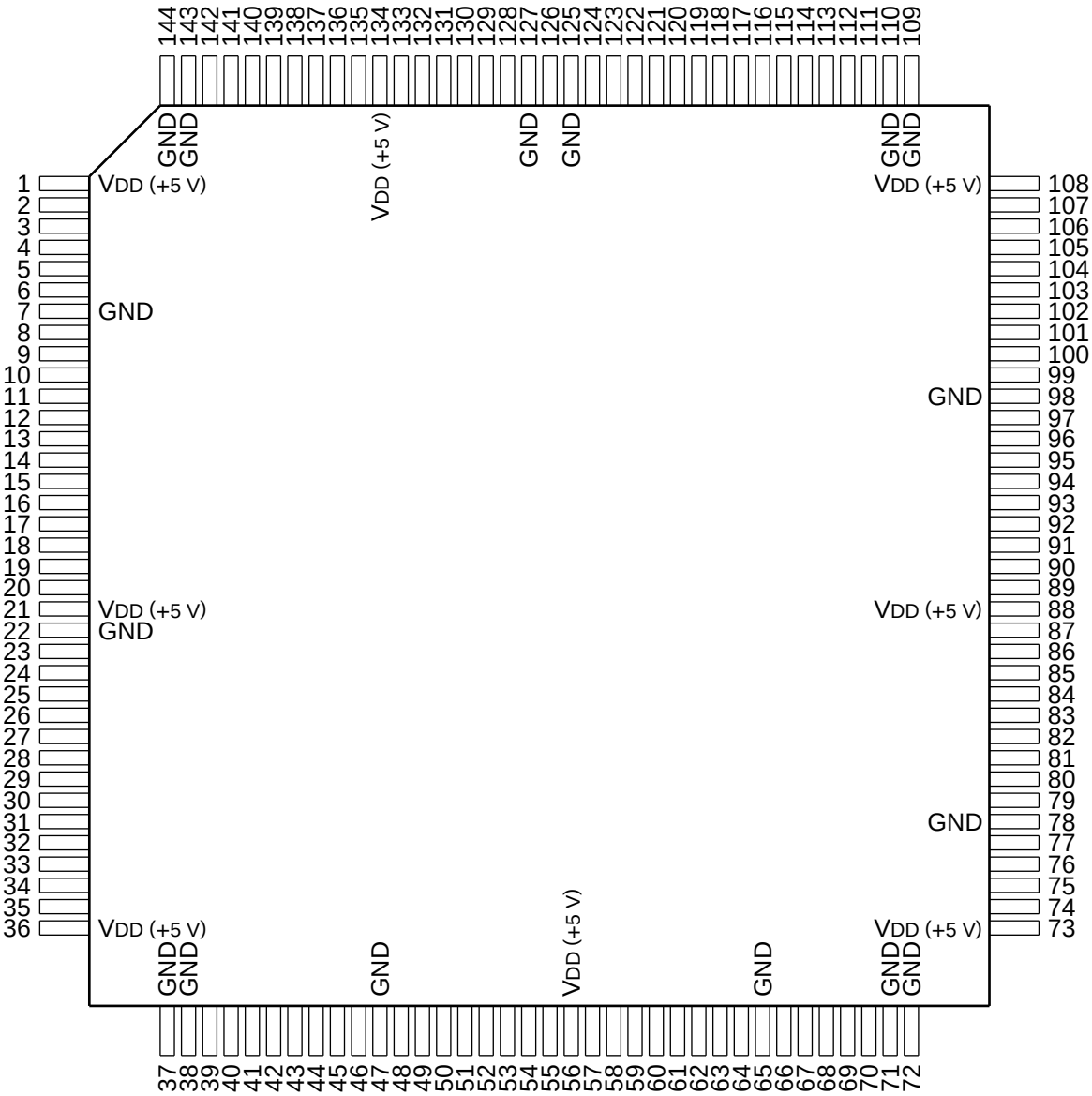
CELL BASED

—TOP VIEW—



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	V_{DD}	37	—	GND	73	—	V_{DD}	109	—	GND
2	I/O	RAD4	38	—	GND	74	I	CS3	110	—	GND
3	I/O	RAD3	39	I/O	D0	75	I	CS4	111	I	OCLK
4	I/O	RAD2	40	I/O	D1	76	I	XAS	112	—	NC
5	I/O	RAD1	41	I/O	D2	77	—	NC	113	I	SW
6	I/O	RAD0	42	I/O	D3	78	—	GND	114	I	XWR2
7	—	GND	43	I/O	D4	79	I/O	BDT0	115	I	XRD2
8	I	XGEN1	44	I/O	D5	80	I/O	BDT1	116	I	XCEN2
9	I	GAD11	45	I/O	D6	81	I/O	BDT2	117	O	FULL
10	I	GAD10	46	I/O	D7	82	I/O	BDT3	118	I	XCCR2
11	I	GAD9	47	—	GND	83	I/O	BDT4	119	I	XCHGE
12	I	GAD8	48	I	A0	84	I/O	BDT5	120	I	XCCR1
13	I/O	GAD7	49	I	A1	85	I/O	BDT6	121	I	XWR1
14	I/O	GAD6	50	I	A2	86	I/O	BDT7	122	I	XRD1
15	I/O	GAD5	51	I	A3	87	I	XBEN2	123	I	XCEN1
16	I/O	GAD4	52	I	A4	88	—	V_{DD}	124	I	XRST
17	I/O	GAD3	53	I	A5	89	I/O	GDT0	125	—	GND
18	I/O	GAD2	54	I	A6	90	I/O	GDT1	126	I	ICLK
19	I/O	GAD1	55	I	A7	91	I/O	GDT2	127	—	GND
20	I/O	GAD0	56	—	V_{DD}	92	I/O	GDT3	128	I	UTEST1
21	—	V_{DD}	57	I	A8	93	I/O	GDT4	129	I	UTEST2
22	—	GND	58	I	A9	94	I/O	GDT5	130	I	TMODE1
23	I	XBEN1	59	I	A10	95	I/O	GDT6	131	I	TMODE2
24	I	BAD11	60	I	A11	96	I/O	GDT7	132	I	TMODE3
25	I	BAD10	61	I	A12	97	I	XGEN2	133	O	TCMP
26	I	BAD9	62	I	A13	98	—	GND	134	—	V_{DD}
27	I	BAD8	63	I	A14	99	I/O	RDT0	135	I	XREN1
28	I/O	BAD7	64	I	A15	100	I/O	RDT1	136	I	RAD11
29	I/O	BAD6	65	—	GND	101	I/O	RDT2	137	I	RAD10
30	I/O	BAD5	66	I	XWRC	102	I/O	RDT3	138	I	RAD9
31	I/O	BAD4	67	I	XRDC	103	I/O	RDT4	139	I	RAD8
32	I/O	BAD3	68	I	XCS0	104	I/O	RDT5	140	I/O	RAD7
33	I/O	BAD2	69	I	XCS1	105	I/O	RDT6	141	I/O	RAD6
34	I/O	BAD1	70	I	XCS2	106	I/O	RDT7	142	I/O	RAD5
35	I/O	BAD0	71	—	GND	107	I	XREN2	143	—	GND
36	—	V_{DD}	72	—	GND	108	—	V_{DD}	144	—	GND