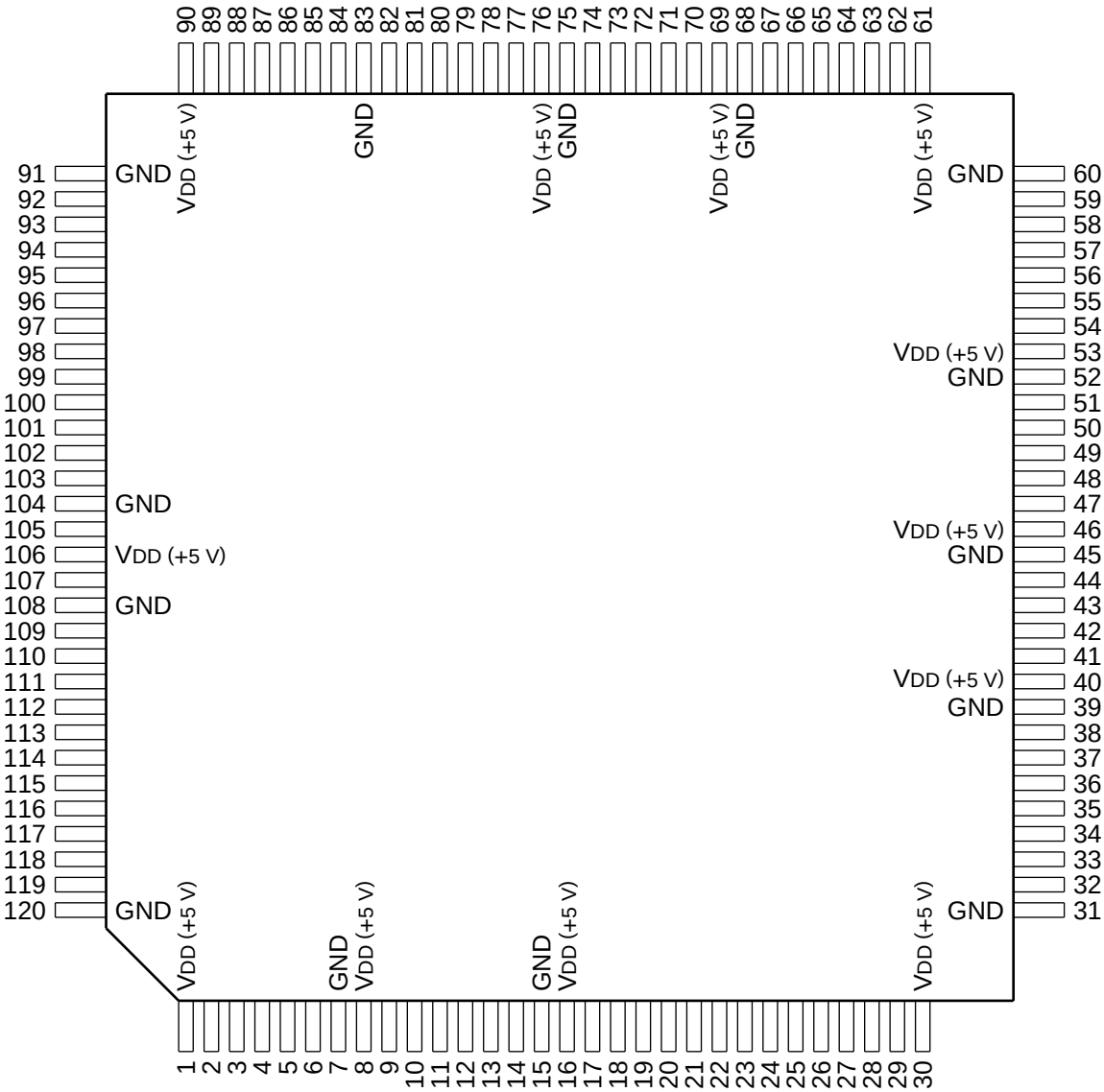
C-MOS GATE ARRAY

—TOP VIEW—



(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	V_{DD}	31	—	GND	61	—	V_{DD}	91	—	GND
2	I/O	D4	32	I	A12	62	O	XWEL	92	I	GI5
3	I/O	D5	33	I	A13	63	O	XWEH	93	I	GI4
4	I/O	D6	34	I	A14	64	O	AR0	94	I	GI3
5	I/O	D7	35	I	A15	65	O	AR1	95	I	GI2
6	I/O	D8	36	I	A16	66	O	AR2	96	I	GI1
7	—	GND	37	I/O	DR15	67	O	AR3	97	I	GI0
8	—	V_{DD}	38	I/O	DR14	68	—	GND	98	I	BI5
9	I/O	D9	39	—	GND	69	—	V_{DD}	99	I	BI4
10	I/O	D10	40	—	V_{DD}	70	O	AR4	100	I	BI3
11	I/O	D11	41	I/O	DR13	71	O	AR5	101	I	BI2
12	I/O	D12	42	I/O	DR12	72	O	AR6	102	I	BI1
13	I/O	D13	43	I/O	DR11	73	O	AR7	103	I	BI0
14	I/O	D14	44	I/O	DR10	74	O	AR8	104	—	GND
15	—	GND	45	—	GND	75	—	GND	105	I	PCLK
16	—	V_{DD}	46	—	V_{DD}	76	—	V_{DD}	106	—	V_{DD}
17	I/O	D15	47	I/O	DR9	77	O	AR9	107	I	SYSCLK
18	I	TEST	48	I/O	DR8	78	O	AR10	108	—	GND
19	I	A1	49	I/O	DR7	79	O	AR11	109	I	XRST
20	I	A2	50	I/O	DR6	80	O	AR12	110	I	XCS0
21	I	A3	51	I/O	DR5	81	O	AR13	111	I	CS1
22	I	A4	52	—	GND	82	O	AR14	112	I	CS2
23	I	A5	53	—	V_{DD}	83	—	GND	113	I	XLWR
24	I	A6	54	I/O	DR4	84	I	RI5	114	I	XHWR
25	I	A7	55	I/O	DR3	85	I	RI4	115	I	XRD
26	I	A8	56	I/O	DR2	86	I	RI3	116	I/O	D0
27	I	A9	57	I/O	DR1	87	I	RI2	117	I/O	D1
28	I	A10	58	I/O	DR0	88	I	RI1	118	I/O	D2
29	I	A11	59	O	XOE	89	I	RI0	119	I/O	D3
30	—	V_{DD}	60	—	GND	90	—	V_{DD}	120	—	GND