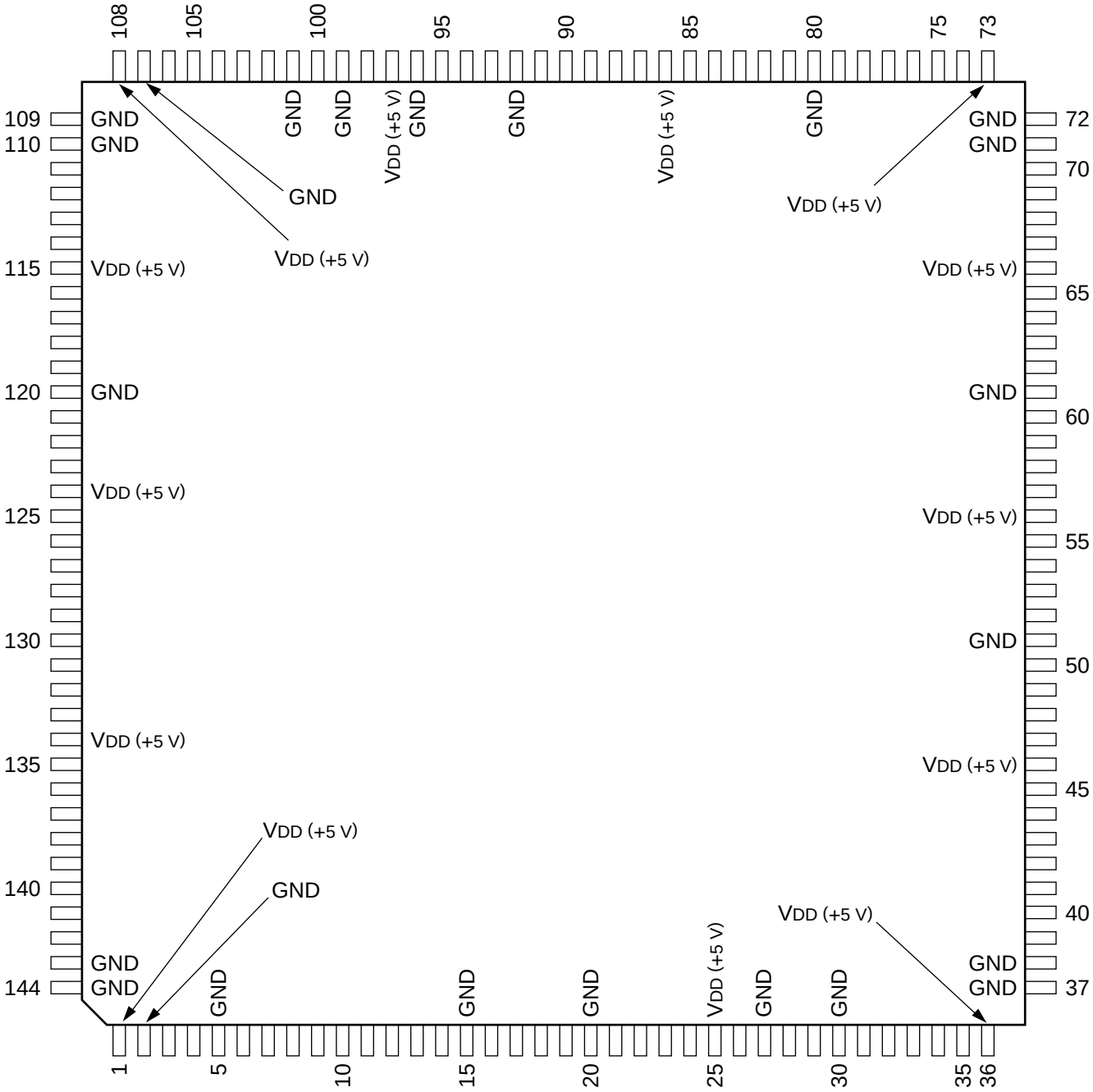
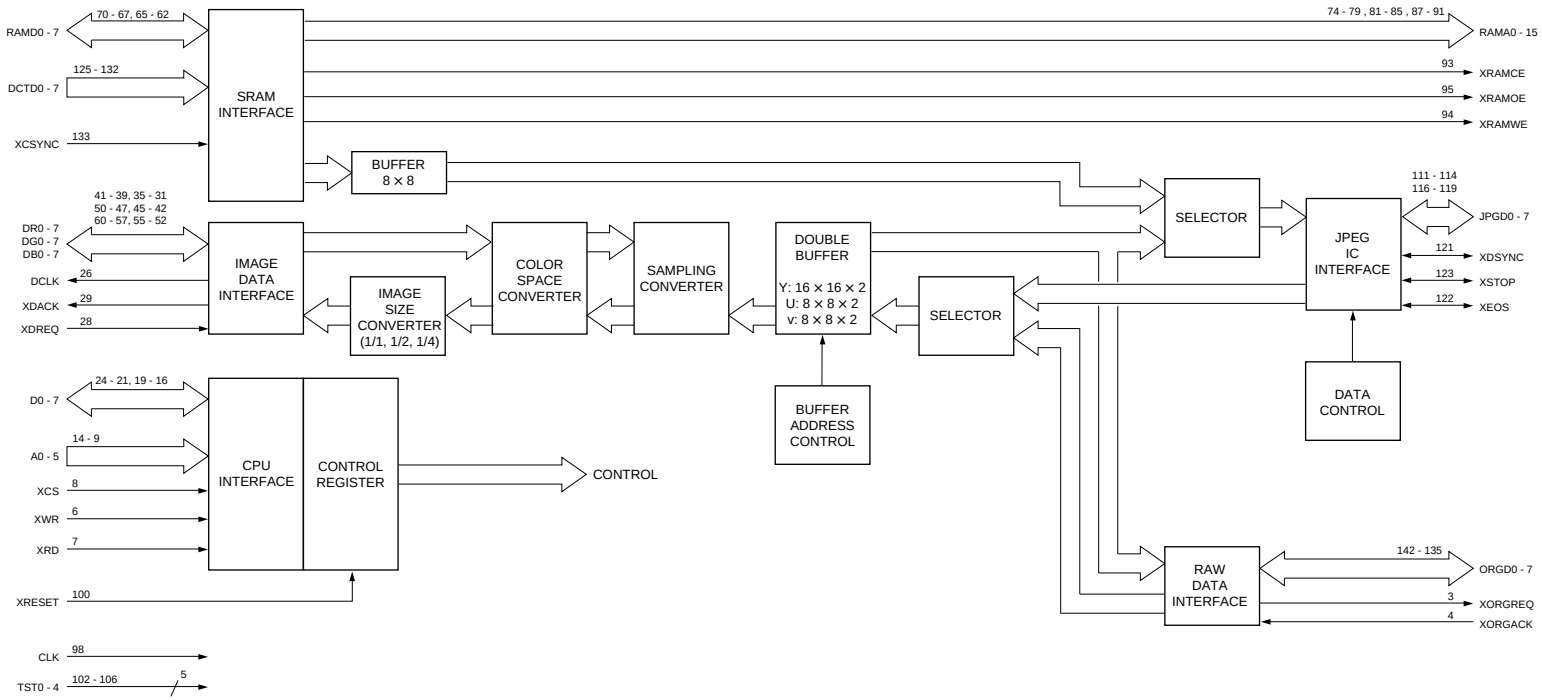
CELL BASED

—TOP VIEW—



(V_{DD} = +5 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V_{DD}	37	—	GND	73	—	V_{DD}	109	—	GND
2	—	GND	38	—	GND	74	O	RAMA0	110	—	GND
3	O	XORGREQ	39	I/O	DR2	75	O	RAMA1	111	I/O	JPGD0
4	I	XORGACK	40	I/O	DR1	76	O	RAMA2	112	I/O	JPGD1
5	—	GND	41	I/O	DR0	77	O	RAMA3	113	I/O	JPGD2
6	I	XWR	42	I/O	DG7	78	O	RAMA4	114	I/O	JPGD3
7	I	XRD	43	I/O	DG6	79	O	RAMA5	115	—	V_{DD}
8	I	XCS	44	I/O	DG5	80	—	GND	116	I/O	JPGD4
9	I	A5	45	I/O	DG4	81	O	RAMA6	117	I/O	JPGD5
10	I	A4	46	—	V_{DD}	82	O	RAMA7	118	I/O	JPGD6
11	I	A3	47	I/O	DG3	83	O	RAMA8	119	I/O	JPGD7
12	I	A2	48	I/O	DG2	84	O	RAMA9	120	—	GND
13	I	A1	49	I/O	DG1	85	O	RAMA10	121	I/O	XDSYNC
14	I	A0	50	I/O	DG0	86	—	V_{DD}	122	I/O	XEOS
15	—	GND	51	—	GND	87	O	RAMA11	123	I/O	XSTOP
16	I/O	D7	52	I/O	DB7	88	O	RAMA12	124	—	V_{DD}
17	I/O	D6	53	I/O	DB6	89	O	RAMA13	125	I	DCTD0
18	I/O	D5	54	I/O	DB5	90	O	RAMA14	126	I	DCTD1
19	I/O	D4	55	I/O	DB4	91	O	RAMA15	127	I	DCTD2
20	—	GND	56	—	V_{DD}	92	—	GND	128	I	DCTD3
21	I/O	D3	57	I/O	DB3	93	O	XRAMCE	129	I	DCTD4
22	I/O	D2	58	I/O	DB2	94	O	XRAMWE	130	I	DCTD5
23	I/O	D1	59	I/O	DB1	95	O	XRAMOE	131	I	DCTD6
24	I/O	D0	60	I/O	DB0	96	—	GND	132	I	DCTD7
25	—	V_{DD}	61	—	GND	97	—	V_{DD}	133	I	XCSYNC
26	O	DCLK	62	I/O	RAMD7	98	I	CLK	134	—	V_{DD}
27	—	GND	63	I/O	RAMD6	99	—	GND	135	I/O	ORGD7
28	I	XDREQ	64	I/O	RAMD5	100	I	XRESET	136	I/O	ORGD6
29	O	XDACK	65	I/O	RAMD4	101	—	GND	137	I/O	ORGD5
30	—	GND	66	—	V_{DD}	102	I	TST0	138	I/O	ORGD4
31	I/O	DR7	67	I/O	RAMD3	103	I	TST1	139	I/O	ORGD3
32	I/O	DR6	68	I/O	RAMD2	104	I	TST2	140	I/O	ORGD2
33	I/O	DR5	69	I/O	RAMD1	105	I	TST3	141	I/O	ORGD1
34	I/O	DR4	70	I/O	RAMD0	106	I	TST4	142	I/O	ORGD0
35	I/O	DR3	71	—	GND	107	—	GND	143	—	GND
36	—	V_{DD}	72	—	GND	108	—	V_{DD}	144	—	GND


RAMD0 - 7
70 - 67, 65 - 62
DCTD0 - 7
125 - 132
XCSYNC
133
SRAM INTERFACE
BUFFER 8 × 8
74 - 79 , 81 - 85 , 87 - 91
RAMA0 - 15
93
XRAMCE
95
XRAMOE
94
XRAMWE
41 - 39, 35 - 31
50 - 47, 45 - 42
60 - 57, 55 - 52
DR0 - 7
DG0 - 7
DB0 - 7
DCLK
26
XDACK
29
XDREQ
28
IMAGE DATA INTERFACE
IMAGE SIZE CONVERTER (1/1, 1/2, 1/4)
COLOR SPACE CONVERTER
SAMPLING CONVERTER
DOUBLE BUFFER
Y: 16 × 16 × 2
U: 8 × 8 × 2
v: 8 × 8 × 2
SELECTOR
SELECTOR
111 - 114
116 - 119
JPEG IC INTERFACE
JPGD0 - 7
121
XDSYNC
123
XSTOP
122
XEOS
DATA CONTROL
BUFFER ADDRESS CONTROL
D0 - 7
24 - 21, 19 - 16
A0 - 5
14 - 9
XCS
8
XWR
6
XRD
7
XRESET
100
CPU INTERFACE
CONTROL REGISTER
CONTROL
CLK
98
TST0 - 4
102 - 106
5
RAW DATA INTERFACE
142 - 135
ORGD0 - 7
3
XORGREQ
4
XORGACK