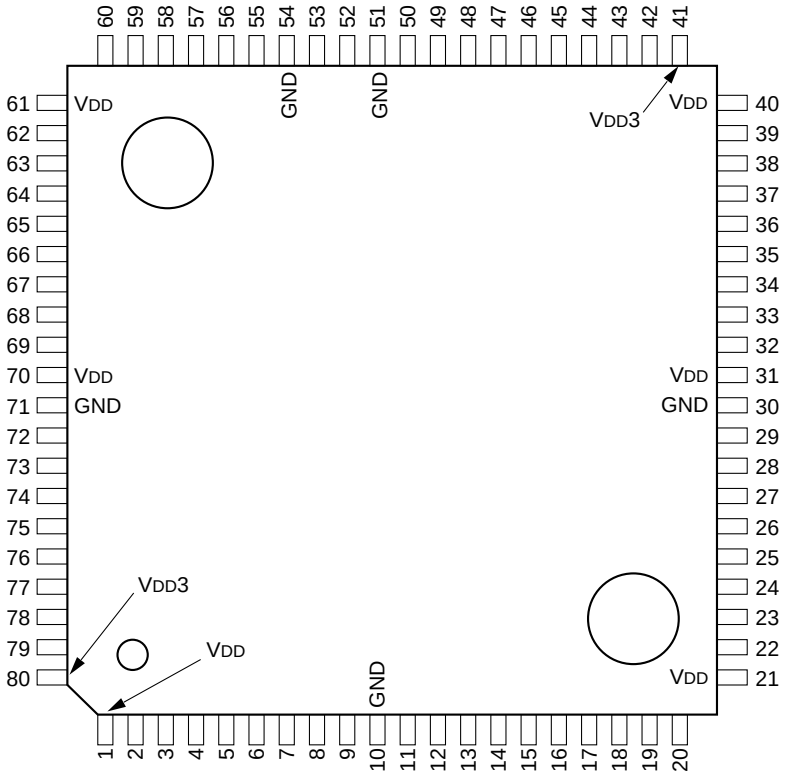
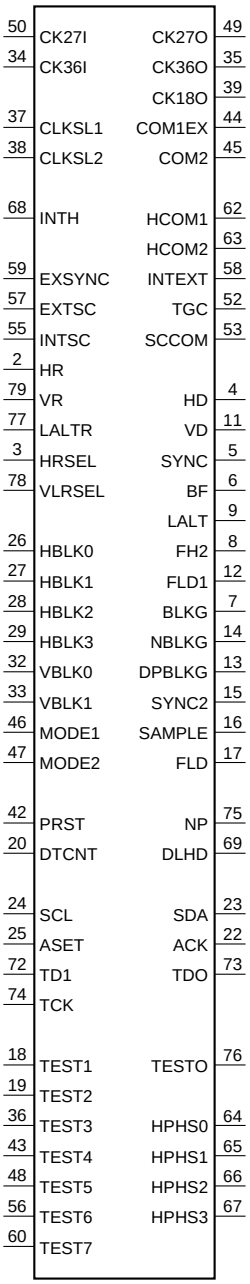
HC-MOS 18 MHz SIGNAL GENERATOR

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	VDD	21	—	VDD	41	—	VDD3	61	—	VDD
2	I	HR	22	O	ACK	42	I	PRST	62	O	HCOM1
3	I	HRSEL	23	I/O	SDA	43	I	TEST4	63	O	HCOM2
4	O	HD	24	I	SCL	44	O	COM1EX	64	I	HPHS0
5	O	SYNC	25	I	ASET	45	O	COM2	65	I	HPHS1
6	O	BF	26	I	HBLK0	46	I	MODE1	66	I	HPHS2
7	O	BLKG	27	I	HBLK1	47	I	MODE2	67	I	HPHS3
8	O	FH2	28	I	HBLK2	48	I	TEST5	68	I	INTH
9	O	LALT	29	I	HBLK3	49	O	CK27O	69	O	DLHD
10	—	GND	30	—	GND	50	I	CK27I	70	—	VDD
11	O	VD	31	—	VDD	51	—	GND	71	—	GND
12	O	FLD1	32	I	VBLK0	52	O	TGC	72	I	TDI
13	O	DPBLKG	33	I	VBLK1	53	O	SCCOM	73	O	TDO
14	O	NBLKG	34	I	CK36I	54	—	GND	74	I	TCK
15	O	SYNC2	35	O	CK36O	55	I	INTSC	75	O	NP
16	O	SAMPLE	36	I	TEST3	56	I	TEST6	76	O	TESTO
17	O	FLD	37	I	CLKSL1	57	I	EXTSC	77	I	LALTR
18	I	TEST1	38	I	CLKSL2	58	O	INTEXT	78	I	VLRSEL
19	I	TEST2	39	O	CK18O	59	I	EXSYNC	79	I	VR
20	I	DTCNT	40	—	VDD	60	I	TEST7	80	—	VDD3



INPUT

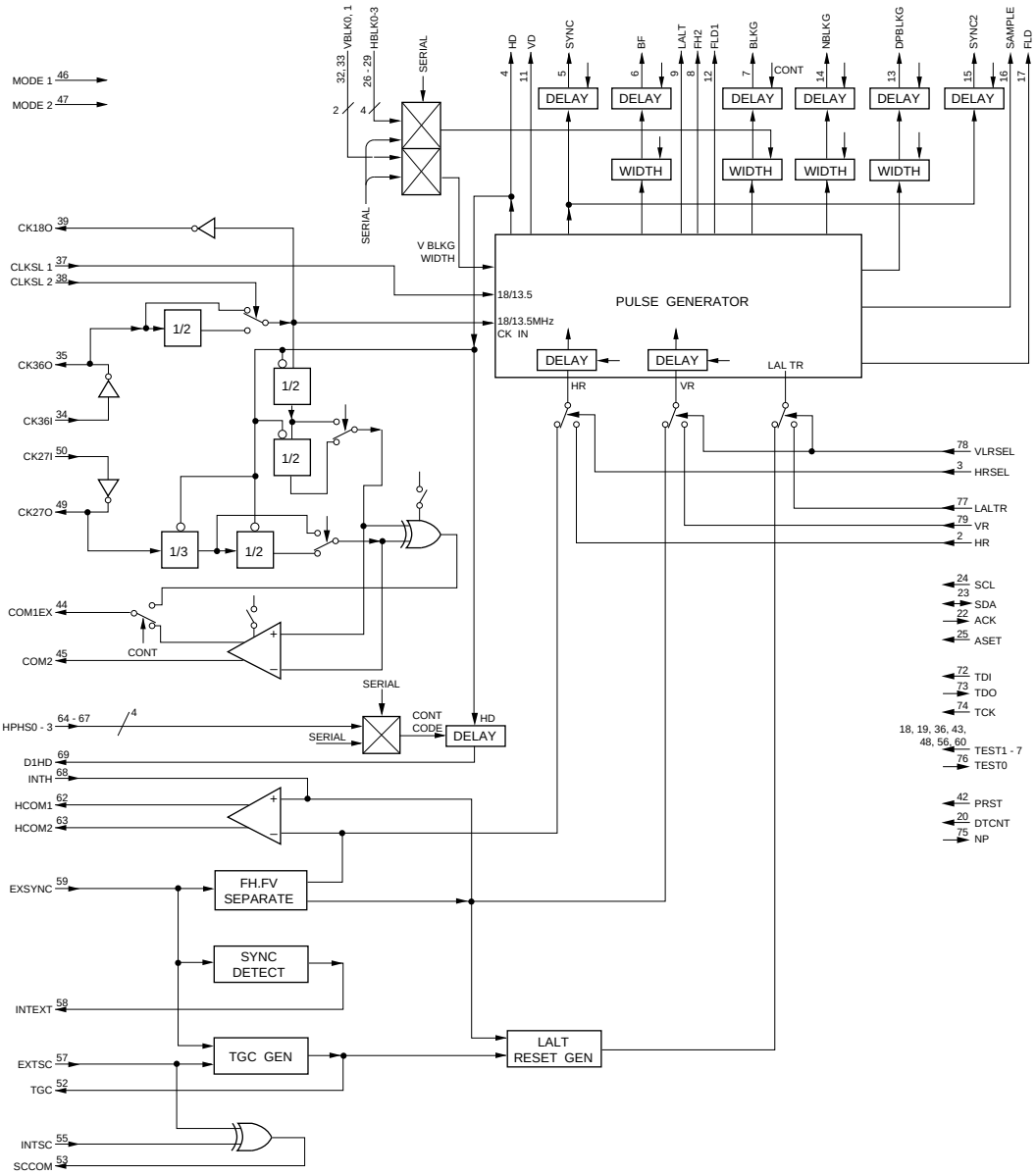
ASET ; ASET OF IIC
CK27I ; 27MHz CLOCK
CK36I ; 36MHz CLOCK
CLKSL1 ; CLOCK FREQUENCY SELECT (LOW = 18MHz, HIGH = 13.5MHz)
CLKSL2 ; CLOCK FREQUENCY SELECT (LOW = 36(27)MHz, HIGH = 18(13.5)MHz)
DTCNT ; VARIOUS DATA SET UP SELECT (LOW = DEFAULT, HIGH = IIC)
EXSYNC ; EXTERNAL SYNC
EXTSC ; EXTERNAL SC
HBLK0 - 3 ; WIDTH OF BLKG H
HPHS0 - 3 ; H-PHASE DATA
HR ; H RESET
HRSEL ; H RESET SELECT
(LOW = FH SEPARATE FROM EXTSYNC, HIGH = HR OF INPUT TERMINAL)
INTH ; AFTER PHASE VARIABLE OF INTERNAL HD AT EXIT
INTSC ; INTERNAL SC
LALTR ; PAL PULSE RESET
MODE1 ; MODE SELECT (LOW = NTSC, HIGH = PAL/PALM)
MODE2 ; MODE SELECT (LOW = NTSC/PALM, HIGH = PAL)
PRST ; POWER ON RESET
SCL ; SOURCE CLOCK
TCK ; TEST CLOCK
TDI ; TEST DATA
TEST1 - 7 ; TEST MODE SET (HIGH = TEST MODE)
VBLK0, 1 ; WIDTH OF BLKG V
VLRSEL ; V RESET/LALT RESET SELECT
(LOW = FV. LALT SEPARATE FROM EXTSYNC,
HIGH = VR. LALTR OF INPUT TERMINAL)
VR ; V RESET

OUTPUT

ACK ; ACK OF IIC
BF ; BF
BLKG ; BLKG
CK18O ; 18 (13.5)MHz CLOCK
CK27O ; 27MHz CLOCK
CK36O ; 36MHz CLOCK
COM1EX ; PHASE COMPARATOR OF CLOCK
(LOW = EDGE COMPARATOR, HIGH = EXOR)
COM2 ; PHASE COMPARATOR OF CLOCK, EDGE COMPARATOR
DLHD ; AFTER PHASE VARIABLE OF INTERNAL HD
DPBLKG ; D1/PRE BLKG (LOW = D1, HIGH = PRE BLKG)
FH2 ; FH2
FLD ; FIEKD ID
FLD1 ; FLD1
HCOM1, 2 ; FH OF SEPARATE FROM EXTSYNC AND
HR OF INPUT TERMINAL PHASE COMPARATOR
HD ; H DRIVE
INTEXT ; EXTERNAL SYNC MODE OR OTHER (LOW = INT, HIGH = EXT)
LALT ; PAL PULSE
NBLKG ; NARROW BLKG
NP ; NTSC/PAL DISCRIMINATE (LOW = NTSC, HIGH = PAL)
SAMPLE ; SAMPLE
SCCOM ; INTSC AND EXTSC COMPARATOR (EXOR)
SYNC ; SYNC
SYNC2 ; SYNC2
TD0 ; TEST DATA
TESO ; TEST MODE
TGC ; TGC
VD ; VD

INPUT/OUTPUT

SDA ; DATA OF IIC


MODE 1 46
MODE 2 47
VBLK0, 1
HBLK0-3
32, 33
26 - 29
SERIAL
HD
VD
SYNC
BF
LALT
FH2
FLD1
BLKG
CONT
NBLKG
DPBLKG
SYNC2
SAMPLE
FLD
DELAY
WIDTH
V BLKG WIDTH
PULSE GENERATOR
18/13.5
18/13.5MHz CK IN
LAL TR
HR
VR
CK18O 39
CLKSL 1 37
CLKSL 2 38
CK36O 35
CK36I 34
CK27I 50
CK27O 49
1/2
1/3
COM1EX 44
COM2 45
CONT
HPHS0 - 3 64 - 67
CODE
D1HD 69
INTH 68
HCOM1 62
HCOM2 63
EXSYNC 59
FH.FV SEPARATE
SYNC DETECT
INTEXT 58
EXTSC 57
TGC GEN
TGC 52
INTSC 55
SCCOM 53
LALT RESET GEN
VLRSEL 78
HRSEL 3
LALTR 77
VR 79
HR 2
SCL 24
SDA 23
ACK 22
ASET 25
TDI 72
TDO 73
TCK 74
18, 19, 36, 43, 48, 56, 60
TEST1 - 7
TEST0 76
PRST 42
DTCNT 20
NP 75