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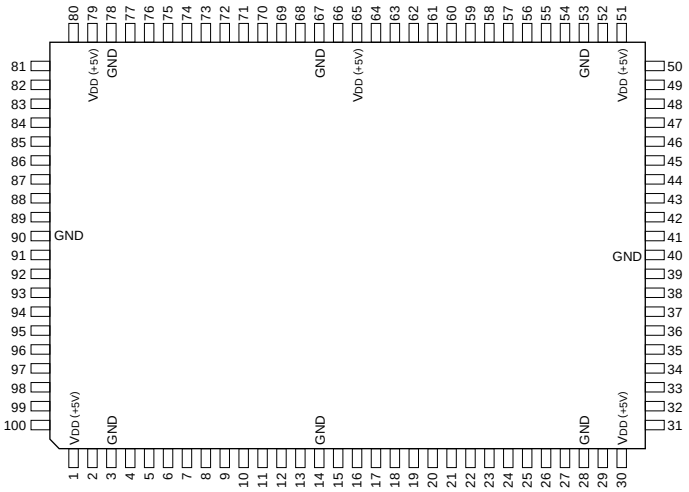
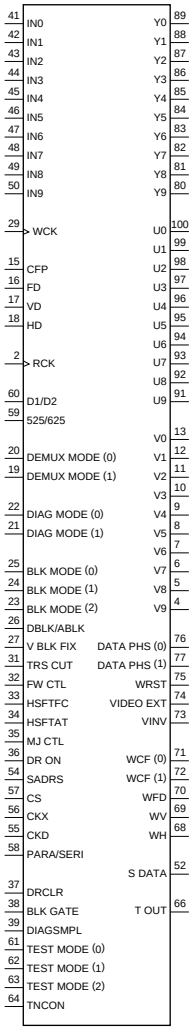
C-MOS DIGITAL VIDEO INPUT PROCESSOR
-TOP VIEW-





(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	VDD	26	I	DBLK ABLK	51	—	VDD	76	O	DATA PHS0
2	I	RCK	27	I	VBLK FIX	52	I/O	SDATA	77	O	DATA PHS1
3	—	GND	28	—	GND	53	—	GND	78	—	GND
4	O	V9	29	I	WCK	54	I	SADRS	79	—	VDD
5	O	V8	30	—	VDD	55	I	CKD	80	O	Y9
6	O	V7	31	I	TRS CUT	56	I	CKX	81	O	Y8
7	O	V6	32	I	FW CTL	57	I	CS	82	O	Y7
8	O	V5	33	I	HSFTFC	58	I	PARA/SERI	83	O	Y6
9	O	V4	34	I	HSFTAT	59	I	525/625	84	O	Y5
10	O	V3	35	I	MJ CTL	60	I	D1/D2	85	O	Y4
11	O	V2	36	I	DR ON	61	I	TEST0	86	O	Y3
12	O	V1	37	I	DR CLR	62	I	TEST1	87	O	Y2
13	O	V0	38	I	BLK GATE	63	I	TEST2	88	O	Y1
14	—	GND	39	I	DIAGSMPL	64	I	TNCON	89	O	Y0
15	I	CFP	40	—	GND	65	—	VDD	90	—	GND
16	I	FD	41	I	IN0	66	O	TOUT	91	O	U9
17	I	VD	42	I	IN1	67	—	GND	92	O	U8
18	I	HD	43	I	IN2	68	O	WH	93	O	U7
19	I	DEMUX MODE1	44	I	IN3	69	O	WV	94	O	U6
20	I	DEMUX MODE0	45	I	IN4	70	O	WFD	95	O	U5
21	I	DIAG MODE1	46	I	IN5	71	O	WCF0	96	O	U4
22	I	DIAG MODE0	47	I	IN6	72	O	WCF1	97	O	U3
23	I	BLK MODE2	48	I	IN7	73	O	VINV	98	O	U2
24	I	BLK MODE1	49	I	IN8	74	O	VIDEO EXT	99	O	U1
25	I	BLK MODE0	50	I	IN9	75	O	WRST	100	O	U0

INPUT

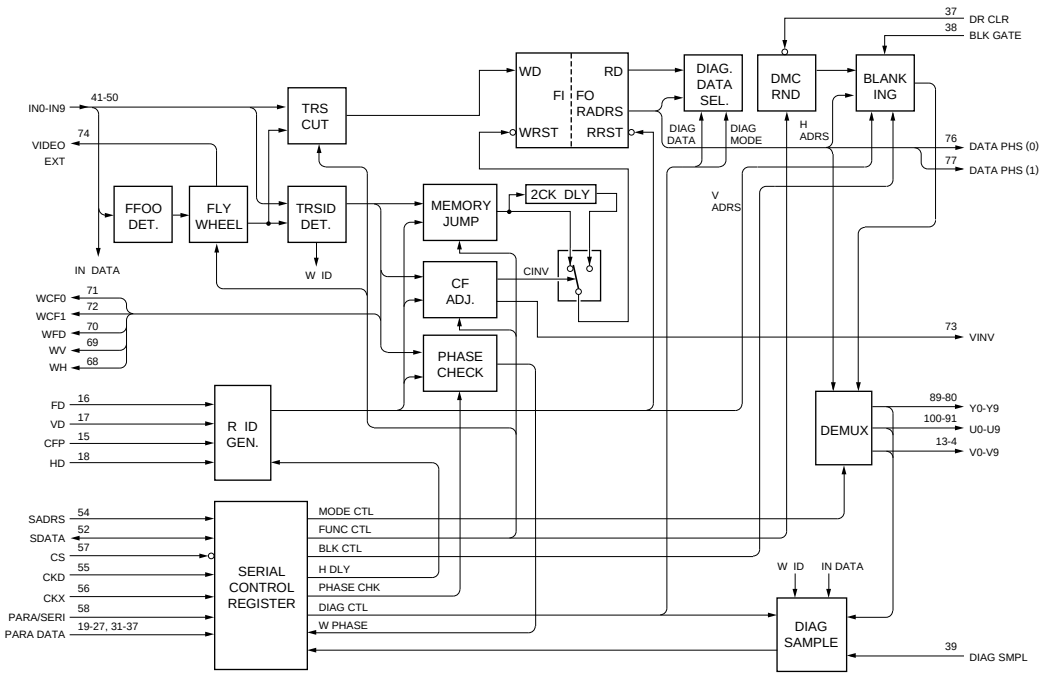
525 / 625	; 525 / 625 SELECT (CONTROL REGISTER PARALLEL DATA)
BLK GATE	; BLANKING SIGNAL
BLK MODE (0-2)	; BLANKING MODE (0-2) (CONTROL REGISTER PARALLEL DATA)
CFP	; SYSTEM CFP (COLOR FRAME PULSE)
CKD	; CONTROL REGISTER SERIAL CLOCK
CKX	; CONTROL REGISTER OPERATION TIMING
CS	; CHIP SELECTOR
D1 / D2	; D1 / D2 SELECT (CONTROL REGISTER PARALLEL DATA)
DBLK / ABLK	; DIGITAL / ANALOG BLANKING SELECT (CONTROL REGISTER PARALLEL DATA)
DEMUX MODE (0-1)	; DEMULTIPLEX MODE (0-1) (CONTROL REGISTER PARALLEL DATA)
DIAG MODE (0-1)	; SELF DIAGNOSIS MODE (0-1) (CONTROL REGISTER PARALLEL DATA)
DIAGSMPL	; SELF DIAGNOSIS SAMPLE PULSE
DRCLR	; DYNAMIC ROUNDING RESET
DR ON	; DYNAMIC ROUNDING ON/OFF (CONTROL REGISTER PARALLEL DATA)
FD	; SYSTEM FD
FW CTL	; FLYWHEEL ON / OFF (CONTROL REGISTER PARALLEL DATA)
HD	; SYSTEM HD
HSFTAT	; AUTO COLOR MATCH (CONTROL REGISTER PARALLEL DATA)
HSFTFC	; FORCED 2CLK DELAY OF TRS (CONTROL REGISTER PARALLEL DATA)
IN (0-9)	; VIDEO SIGNAL (0-9)
MJ CTL	; MEMORY JUMP ON/OFF (CONTROL REGISTER PARALLEL DATA)
PARA / SERI	; PARALLEL SERIAL SELECT
RCK	; FIFO READ CLOCK
SADRS	; CONTROL REGISTER SIGNAL ADDRESS
TRS CUT	; TRS CANCELLATION (CONTROL REGISTER PARALLEL DATA)
V BLK FIX	; FIXED V BLANKING (CONTROL REGISTER PARALLEL DATA)
VD	; SYSTEM VD
WCK	; FIFO WRITE CLOCK

OUTPUT

DATA PHS (0-1)	; VIDEO PHASE INFORMATION (0-1)
T OUT	; TEST OUT (SET OPEN)
VIDEO EXT	; VIDEO CHECK FLAG
VINV	; V INVERT (D2 PAL)
WCF (0-1)	; DETECTED CF (0-1)
WFD	; DETECTED FD
WH	; DETECTED HD
WRST	; FIFO RESET PULSE
WV	; DETECTED VD

INPUT/OUTPUT

SDATA	; CONTROL REGISTER SERIAL DATA


37
DR CLR
38
BLK GATE
IN0-IN9
41-50
VIDEO
EXT
74
TRS
CUT
WD
RD
FI
FO
RADRS
WRST
RRST
DIAG.
DATA
SEL.
DMC
RND
BLANK
ING
DIAG
DATA
DIAG
MODE
H
ADRS
76
DATA PHS (0)
77
DATA PHS (1)
FFOO
DET.
FLY
WHEEL
TRSID
DET.
MEMORY
JUMP
2CK DLY
V
ADRS
IN DATA
W ID
CF
ADJ.
CINV
WCF0
WCF1
WFD
WV
WH
71
72
70
69
68
PHASE
CHECK
73
VINV
FD
VD
CFP
HD
16
17
15
18
R ID
GEN.
DEMUX
89-80
Y0-Y9
100-91
U0-U9
13-4
V0-V9
SADRS
SDATA
CS
CKD
CKX
PARA/SERI
PARA DATA
54
52
57
55
56
58
19-27, 31-37
SERIAL
CONTROL
REGISTER
MODE CTL
FUNC CTL
BLK CTL
H DLY
PHASE CHK
DIAG CTL
W PHASE
W ID
IN DATA
DIAG
SAMPLE
39
DIAG SMPL