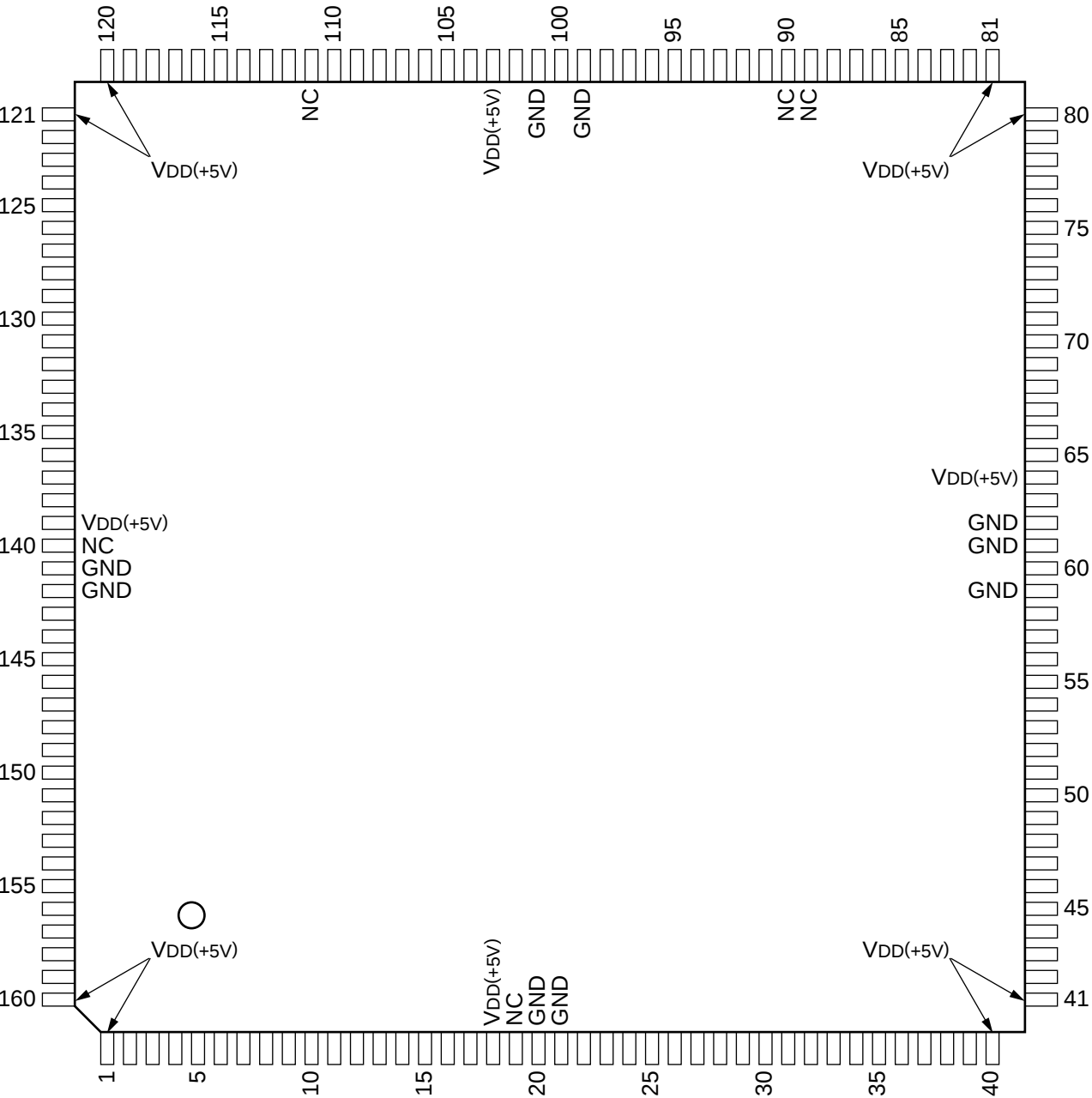

C-MOS VIDEO MODIFIER
-TOP VIEW-



(VDD = +5V)

133	IN0 0	OUT0 0	149
132	IN0 1	OUT0 1	148
131	IN0 2	OUT0 2	147
130	IN0 3	OUT0 3	146
129	IN0 4	OUT0 4	145
128	IN0 5	OUT0 5	144
127	IN0 6	OUT0 6	143
126	IN0 7	OUT0 7	138
125	IN0 8	OUT0 8	137
124	IN0 9	OUT0 9	136
123	IN0 A	OUT0 A	135
122	IN0 B	OUT0 B	134
3	IN1 0	OUT1 0	28
2	IN1 1	OUT1 1	27
159	IN1 2	OUT1 2	26
158	IN1 3	OUT1 3	25
157	IN1 4	OUT1 4	24
156	IN1 5	OUT1 5	23
155	IN1 6	OUT1 6	22
154	IN1 7	OUT1 7	17
153	IN1 8	OUT1 8	16
152	IN1 9	OUT1 9	15
151	IN1 A	OUT1 A	14
150	IN1 B	OUT1 B	13
31	IN2 0	OUT2 0	70
30	IN2 1	OUT2 1	69
29	IN2 2	OUT2 2	68
12	IN2 3	OUT2 3	67
11	IN2 4	OUT2 4	66
10	IN2 5	OUT2 5	65
9	IN2 6	OUT2 6	58
8	IN2 7	OUT2 7	57
7	IN2 8	OUT2 8	56
6	IN2 9	OUT2 9	55
5	IN2 A	OUT2 A	54
4	IN2 B	OUT2 B	53
45	IN3 0	OUT3 0	110
44	IN3 1	OUT3 1	109
43	IN3 2	OUT3 2	108
42	IN3 3	OUT3 3	107
39	IN3 4	OUT3 4	106
38	IN3 5	OUT3 5	105
37	IN3 6	OUT3 6	104
36	IN3 7	OUT3 7	98
35	IN3 8	OUT3 8	97
34	IN3 9	OUT3 9	96
33	IN3 A	OUT3 A	95
32	IN3 B	OUT3 B	94
75	IN4 0	DT1YO	92
74	IN4 1	DT1CO	91
73	IN4 2	DT2O	93
72	IN4 3	OE0	76
71	IN4 4	OE1	77
52	IN4 5	OE2	78
51	IN4 6	OE3	79
50	IN4 7	DT1I	82
49	IN4 8	DT2I	83
48	IN4 9	DT1I	82
47	IN4 A	DT2I	83
46	IN4 B	DT1I	82
117	CTIM	TN IN	88
102	SDAT	TSTO	118
112	SADD		
60	CK		
63	CKS		
100	CKD		
113	CKX		
118	RST		
116	CS0		
115	CS1		
114	CS2		
84	LD1		
86	LD2		
85	EN1		
87	EN2		

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VDD	41	—	VDD	81	—	VDD	121	—	VDD
2	I	IN1 1	42	I	IN3 3	82	I	DT1I	122	I	IN0 B
3	I	IN1 0	43	I	IN3 2	83	I	DT2I	123	I	IN0 A
4	I	IN2 B	44	I	IN3 1	84	I	LD1	124	I	IN0 9
5	I	IN2 A	45	I	IN3 0	85	I	EN1	125	I	IN0 8
6	I	IN2 9	46	I	IN4 B	86	I	LD2	126	I	IN0 7
7	I	IN2 8	47	I	IN4 A	87	I	EN2	127	I	IN0 6
8	I	IN2 7	48	I	IN4 9	88	I	TN IN	128	I	IN0 5
9	I	IN2 6	49	I	IN4 8	89	—	NC	129	I	IN0 4
10	I	IN2 5	50	I	IN4 7	90	—	NC	130	I	IN0 3
11	I	IN2 4	51	I	IN4 6	91	O	DT1CO	131	I	IN0 2
12	I	IN2 3	52	I	IN4 5	92	O	DT1YO	132	I	IN0 1
13	O	OUT1 B	53	O	OUT2 B	93	O	DT2O	133	I	IN0 0
14	O	OUT1 A	54	O	OUT2 A	94	O	OUT3 B	134	O	OUT0 B
15	O	OUT1 9	55	O	OUT2 9	95	O	OUT3 A	135	O	OUT0 A
16	O	OUT1 8	56	O	OUT2 8	96	O	OUT3 9	136	O	OUT0 9
17	O	OUT1 7	57	O	OUT2 7	97	O	OUT3 8	137	O	OUT0 8
18	—	VDD	58	O	OUT2 6	98	O	OUT3 7	138	O	OUT0 7
19	—	NC	59	—	GND	99	—	GND	139	—	VDD
20	—	GND	60	I	CK	100	I	CKD	140	—	NC
21	—	GND	61	—	GND	101	—	GND	141	—	GND
22	O	OUT1 6	62	—	GND	102	I/O	SDAT	142	—	GND
23	O	OUT1 5	63	I	CKS	103	—	VDD	143	O	OUT0 6
24	O	OUT1 4	64	—	VDD	104	O	OUT3 6	144	O	OUT0 5
25	O	OUT1 3	65	O	OUT2 5	105	O	OUT3 5	145	O	OUT0 4
26	O	OUT1 2	66	O	OUT2 4	106	O	OUT3 4	146	O	OUT0 3
27	O	OUT1 1	67	O	OUT2 3	107	O	OUT3 3	147	O	OUT0 2
28	O	OUT1 0	68	O	OUT2 2	108	O	OUT3 2	148	O	OUT0 1
29	I	IN2 2	69	O	OUT2 1	109	O	OUT3 1	149	O	OUT0 0
30	I	IN2 1	70	O	OUT2 0	110	O	OUT3 0	150	I	IN1 B
31	I	IN2 0	71	I	IN4 4	111	—	NC	151	I	IN1 A
32	I	IN3 B	72	I	IN4 3	112	I	SADD	152	I	IN1 9
33	I	IN3 A	73	I	IN4 2	113	I	CKX	153	I	IN1 8
34	I	IN3 9	74	I	IN4 1	114	I	CS2	154	I	IN1 7
35	I	IN3 8	75	I	IN4 0	115	I	CS1	155	I	IN1 6
36	I	IN3 7	76	I	OE0	116	I	CS0	156	I	IN1 5
37	I	IN3 6	77	I	OE1	117	I	CTIM	157	I	IN1 4
38	I	IN3 5	78	I	OE2	118	O	TSTO	158	I	IN1 3
39	I	IN3 4	79	I	OE3	119	I	RST	159	I	IN1 2
40	—	VDD	80	—	VDD	120	—	VDD	160	—	VDD

INPUT

CK ; SYSTEM CLOCK
 CKD ; CLOCK FOR CS0, CS1, CS2, SADD, SDAT
 CKS ; CLOCK FOR SAMPLE AND HOLD CIRCUIT IN OUT1
 CKX ; TIMING SIGNAL FOR SERIAL CONTROL EXECUTION
 CS0-CS2 ; CHIP SELECT
 CTIM ; COLOR TIMING SPECIFIED
 DT1I, DT2I ; SAMPLE PULSE FOR SAMPLE AND HOLD CIRCUIT IN OUT1, OUT2
 EN1, EN2 ; NAMADD1, NAMADD2 CIRCUIT ENABLE (IN COUNTER MODE)
 IN0 0-IN0 B, IN1 0-IN1 B, IN2 0-IN2 B, IN3 0-IN3 B, IN4 0-IN4 B
 ; DATA
 LD1, LD2 ; NAMADD1, NAMADD2 CIRCUIT LOAD PIN (IN COUNTER MODE)
 OE0-OE3 ; OUTPUT ENABLE FOR OUT0, OUT1, OUT2, OUT3
 SADD ; SERIAL ADDRESS
 RST ; POWER RESET
 TN IN ; TEST TERMINAL

OUTPUT

DT1YO, DT1CO, DT2O
 ; SAMPLE PULSE
 OUT0 0-OUT0 B, OUT1 0-OUT1 B, OUT2 0-OUT2 B, OUT3 0-OUT3 B
 ; DATA
 TSTO ; TEST TERMINAL

INPUT/OUTPUT

SDAT ; SERIAL DATA

