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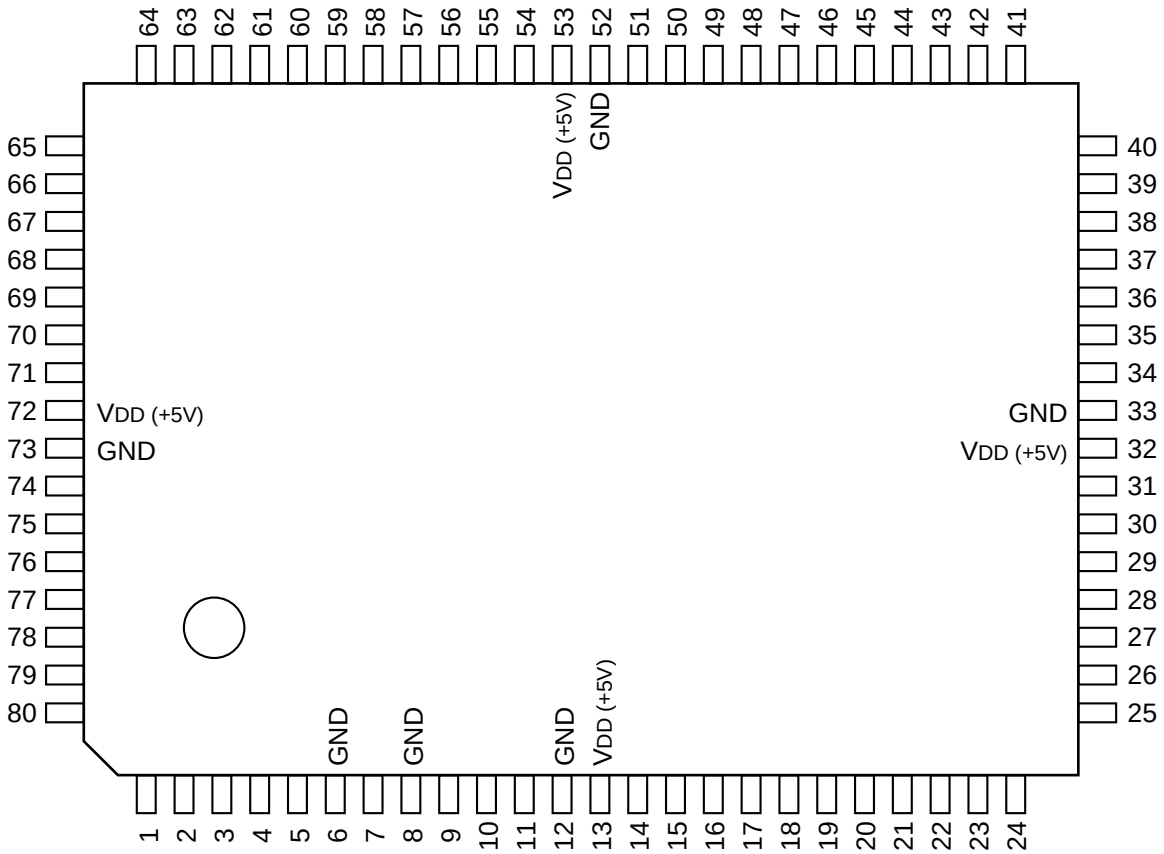
CXD8278AQ(1/4)
IL00

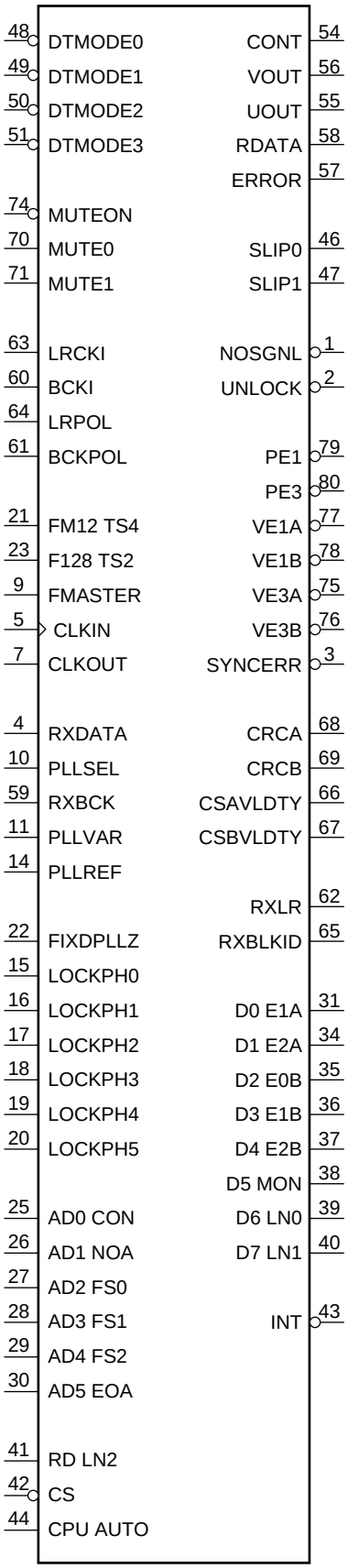
C-MOS DIGITAL AUDIO SIGNAL (AES/EBU) DECODER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	$\overline{\text{NOSGNL}}$	21	I/O	FM12 TS4	41	I/O	RD LN2	61	I	BCKPOL
2	O	$\overline{\text{UNLOCK}}$	22	I/O	FIXDPLLZ	42	I	$\overline{\text{CS}}$	62	O	RXLR
3	O	$\overline{\text{SYNCERR}}$	23	I/O	F128 TS2	43	O	$\overline{\text{INT}}$	63	I	LRCKI
4	I	RXDATA	24	I	TST3	44	I	CPU AUTO	64	I	LRPOL
5	I	CLKIN	25	I/O	AD0 CON	45	I	TST1	65	O	RXBLKID
6	—	GND	26	I/O	AD1 NOA	46	O	SLIP0	66	O	CSAVLDTY
7	O	CLKOUT	27	I/O	AD2 FS0	47	O	SLIP1	67	O	CSBVLDTY
8	—	GND	28	I/O	AD3 FS1	48	I	DTMODE0	68	O	CRCA
9	O	FMASTER	29	I/O	AD4 FS2	49	I	DTMODE1	69	O	CRCB
10	I	PLLSEL	30	I/O	AD5 E0A	50	I	DTMODE2	70	I	MUTE0
11	O	PLLVAR	31	O	D0 E1A	51	I	DTMODE3	71	I	MUTE1
12	—	GND	32	—	V_{DD}	52	—	GND	72	—	V_{DD}
13	—	V_{DD}	33	—	GND	53	—	V_{DD}	73	—	GND
14	O	PLLREF	34	O	D1 E2A	54	O	COUT	74	I	$\overline{\text{MUTEON}}$
15	I/O	LOCKPH0	35	O	D2 E0B	55	O	UOUT	75	O	$\overline{\text{VE3A}}$
16	I/O	LOCKPH1	36	O	D3 E1B	56	O	VOUT	76	O	$\overline{\text{VE3B}}$
17	I/O	LOCKPH2	37	O	D4 E2B	57	O	ERROR	77	O	$\overline{\text{VE1A}}$
18	I/O	LOCKPH3	38	O	D5 MON	58	O	RDATA	78	O	$\overline{\text{VE1B}}$
19	I/O	LOCKPH4	39	O	D6 LN0	59	O	RXBCK	79	O	$\overline{\text{PE1}}$
20	I/O	LOCKPH5	40	O	D7 LN1	60	I	BCKI	80	O	$\overline{\text{PE3}}$

CXD8278AQ(2/4)



INPUT

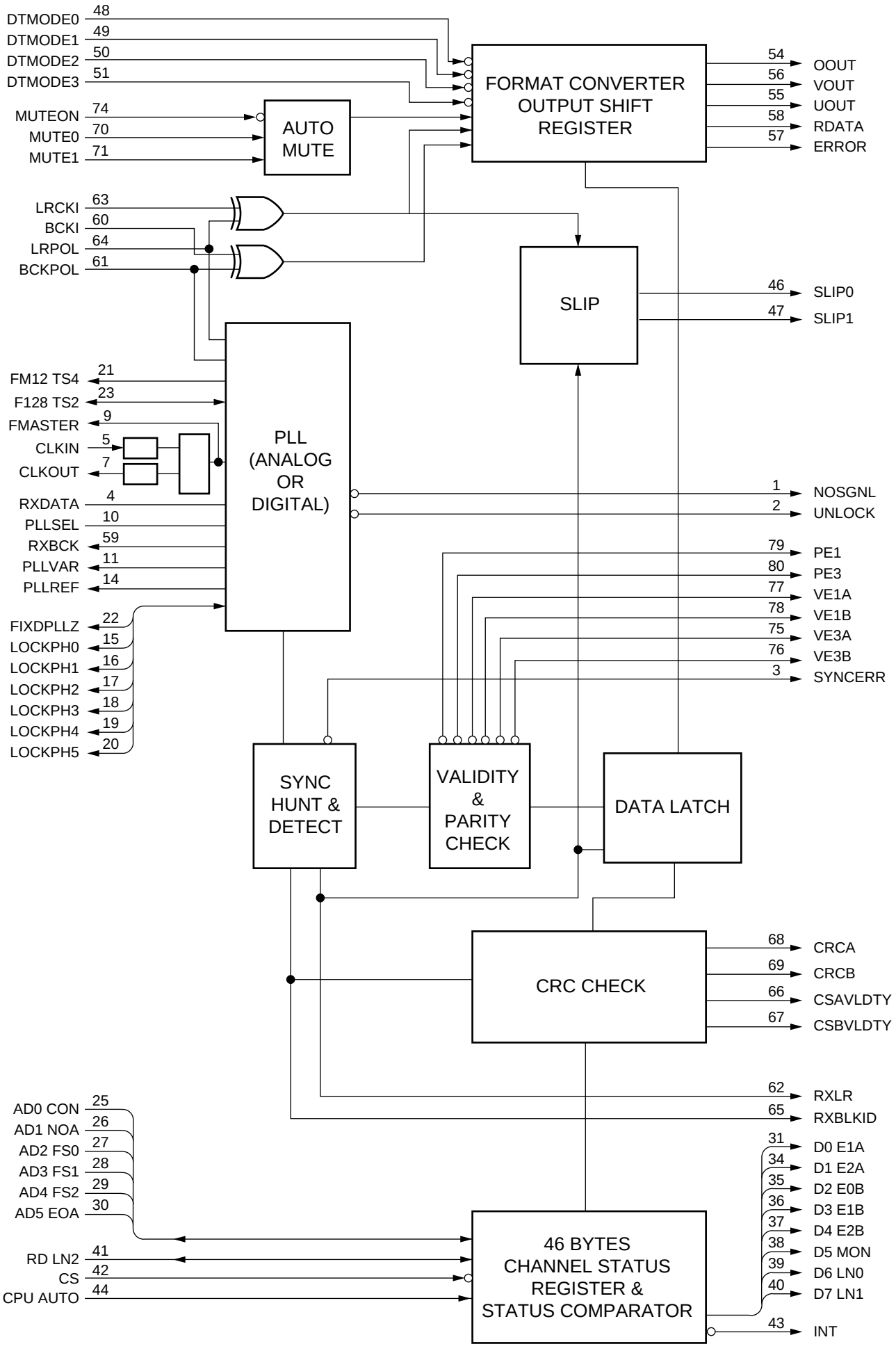
BCKI	;	REFERENCE BIT CLOCK (64/32Fs)
BCKPOL	;	POLARITY SWITCHING SIGNAL OF BCKI (PIN NO.60) AND RXBCK (PIN NO.59)
CLKIN	;	MASTER CLOCK OSCILLATOR INPUT AT DIGITAL PLL
CPU AUTO	;	SELECTS CPU INTERFACE OR AUTO INTERFACE.
	;	("H" : AUTO INTERFACE, "L" : CPU INTERFACE)
$\overline{CS}$	;	CHIP SELECT SIGNAL (INPUT FOR CHANNEL STATUS REGISTER) ("L" : SELECT)
DTMODE0-3	;	OUTPUT FORMAT SPECIFYING CODE OF RDATA SIGNAL (PIN NO.58)
LRCKI	;	REFERENCE L/R CLOCK INPUT (Fs PERIOD)
LRPOL	;	POLARITY SWITCHING SIGNAL OF LRCKI (PIN NO.63) AND RXLR (PIN NO.62)
MUTE0, 1	;	RDATA (PIN NO.58) MUTE PERIOD SETTING CODE
$\overline{MUTEON}$	;	"L" : AUDIO OUTPUT BE FORCIBLY MUTE ON FOR A CERTAIN PERIOD
PLLSEL	;	"L" : ANALOG PLL. "H" : DIGITAL PLL
RXDATA	;	AES/EBU INPUT
TST1	;	TEST INPUT (NORMALLY FIXED TO "L")
TST3	;	TEST PIN (FIXED TO "L")

OUTPUT

CLKOUT	;	MASTER CLOCK OSCILLATOR OUTPUT AT DIGITAL PLL
COUT	;	C BIT STATUS SIGNAL EXTRACTED FROM AES/EBU INPUT SIGNAL.
CRCA, CRCB	;	OUTPUTS THE RESULT OF CHANNEL STATUS CRC CHECK OF SUBFRAME A AND B AT ERROR OCCURRING
CSAVLDTY, CSBVLDTY	;	SUBFRAME A AND B CHANNEL STATUS
D0 E1A	;	SUBFRAME A CHANNEL STATUS (CPU AUTO : "H")
D1 E2A	;	SUBFRAME A CHANNEL STATUS (CPU AUTO : "H")
D2 E0B	;	SUBFRAME B CHANNEL STATUS (CPU AUTO : "H")
D3 E1B	;	SUBFRAME B CHANNEL STATUS (CPU AUTO : "H")
D4 E2B	;	SUBFRAME B CHANNEL STATUS (CPU AUTO : "H")
D5 MON	;	SUBFRAME A CHANNEL STATUS (CPU AUTO : "H")
D6 LN0	;	SUBFRAME A/B CHANNEL STATUS (CPU AUTO : "H")
D7 LN1	;	SUBFRAME A/B CHANNEL STATUS (CPU AUTO : "H")
ERROR	;	ERROR INFORMATION OUTPUT (PARITY, SLIP ERROR , etc.) IN SERIAL
FMASTER	;	MASTER CLOCK OUTPUT
$\overline{INT}$	;	INTERRUPTION SIGNAL OUTPUT
$\overline{NOSGNL}$	;	NO SIGNAL DETECTION
$\overline{PE1}$	;	PARITY ERROR DETECTION OUTPUT (1 SUBFRAM)
$\overline{PE3}$	;	PARITY ERROR DETECTION OUTPUT (3 SUBFRAMS CONTINUOUSLY)
PLLREF	;	RXDATA SYNC DETECTION
PLLVAR	;	ANALOG PLL MASTER CLOCK 1/256 (2Fs) SIGNAL
RDATA	;	AES/EBU INPUT SIGNAL DEMODULATED SIGNAL OUTPUT
RXBCK	;	BIT CLOCK OUTPUT GENERATED FROM AES/EBU INPUT SIGNAL
RXBLKID	;	BLOCK ID SIGNAL
RXLR	;	REFERENCE L/R CLOCK OUTPUT (Fs PERIOD)
SLIP0, SLIP1	;	DATA SLIP DETECTION
$\overline{SYNCERR}$	;	SYNC ERROR DETECTION OUTPUT.
$\overline{UNLOCK}$	;	DIGITAL PLL UNLOCK DETECTION OUTPUT.
$\overline{UOUT}$	;	U BIT (USER DATA BIT) STATUS SIGNAL EXTRACTED FROM RXDATA SIGNAL
$\overline{VE1A}$	;	VALIDITY ERROR DETECTION OUTPUT (ONE SUBFRAM A).
$\overline{VE1B}$	;	VALIDITY ERROR DETECTION OUTPUT (ONE SUBFRAM B).
VE3A	;	VALIDITY ERROR DETECTION OUTPUT (3FRAMS CONTINUOUSLY FOR SUBFRAM A)
VE3B	;	VALIDITY ERROR DETECTION OUTPUT (3FRAMS CONTINUOUSLY FOR SUBFRAM B)
VOUT	;	V BIT (VALIDITY BIT) STATUS SIGNAL EXTRACTED FROM RXDATA SIGNAL

INPUT/OUTPUT

AD0 CON	;	CHANNEL STATUS (CPU AUTO : "H")
AD1 NOA	;	CHANNEL STATUS (CPU AUTO : "H")
AD2 FS0	;	CHANNEL STATUS (CPU AUTO : "H")
AD3 FS1	;	CHANNEL STATUS (CPU AUTO : "H")
AD4 FS2	;	CHANNEL STATUS (CPU AUTO : "H")
AD5 EOA	;	SUBFRAME A CHANNEL STATUS (CPU AUTO : "H")
F128 TS2	;	OUTPUTS 128Fs OF DIGITAL PLL.
FIXDPLL	;	PLLSEL : "H", DIGITAL PLL OPERATION MODE SELECTION SIGNAL ("N" : NARROW MODE, "H" : WIDE MODE)
FM12 TS4	;	1/2 MCK OUTPUT
LOCKPH0-5	;	PLLSEL : "H", FIXDPLL : "H" OPERATION PERIOD SETTING DATA INPUT AT NARROW MODE (DIGITAL PLL MODE)
RD LN2	;	SUBFRAME A/B CHANNEL STATUS (CPU AUTO : "H")


DTMODE0
48
DTMODE1
49
DTMODE2
50
DTMODE3
51
MUTEON
74
MUTE0
70
MUTE1
71
AUTO MUTE
FORMAT CONVERTER OUTPUT SHIFT REGISTER
54
OOUT
56
VOUT
55
UOUT
58
RDATA
57
ERROR
LRCKI
63
BCKI
60
LRPOL
64
BCKPOL
61
SLIP
46
SLIP0
47
SLIP1
FM12 TS4
21
F128 TS2
23
FMASTER
9
CLKIN
5
CLKOUT
7
RXDATA
4
PLLSEL
10
RXBCK
59
PLLVAR
11
PLLREF
14
PLL (ANALOG OR DIGITAL)
1
NOSGNL
2
UNLOCK
79
PE1
80
PE3
77
VE1A
78
VE1B
75
VE3A
76
VE3B
3
SYNCERR
FIXDPLLZ
22
LOCKPH0
15
LOCKPH1
16
LOCKPH2
17
LOCKPH3
18
LOCKPH4
19
LOCKPH5
20
SYNC HUNT & DETECT
VALIDITY & PARITY CHECK
DATA LATCH
CRC CHECK
68
CRCA
69
CRCB
66
CSAVLDTY
67
CSBVLDTY
62
RXLR
65
RXBLKID
AD0 CON
25
AD1 NOA
26
AD2 FS0
27
AD3 FS1
28
AD4 FS2
29
AD5 EOA
30
RD LN2
41
CS
42
CPU AUTO
44
46 BYTES CHANNEL STATUS REGISTER & STATUS COMPARATOR
31
D0 E1A
34
D1 E2A
35
D2 E0B
36
D3 E1B
37
D4 E2B
38
D5 MON
39
D6 LN0
40
D7 LN1
43
INT