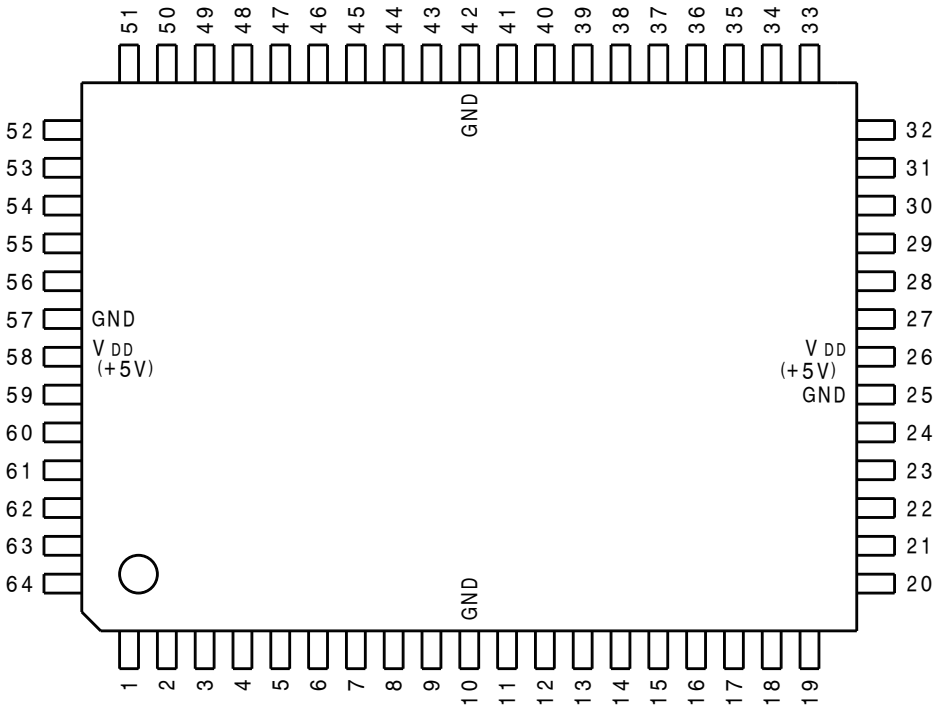
****

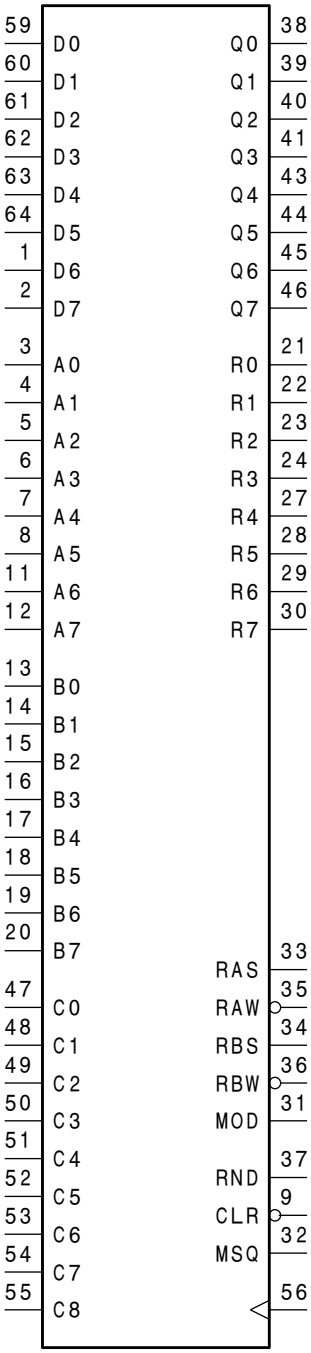
C-MOS LINEAR INTERPOLATION

-TOP VIEW-



(V_{DD}=+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGANL	PIN No.	I/O	SIGNAL
1	I	D6	17	I	B4	33	I	RAS	49	I	C2
2	I	D7	18	I	B5	34	I	RBS	50	I	C3
3	I	A0	19	I	B6	35	I	RAW	51	I	C4
4	I	A1	20	I	B7	36	I	RBW	52	I	C5
5	I	A2	21	O	R0	37	I	RND	53	I	C6
6	I	A3	22	O	R1	38	O	Q0	54	I	C7
7	I	A4	23	O	R2	39	O	Q1	55	I	C8
8	I	A5	24	O	R3	40	O	Q2	56	I	CK
9	I	CLR	25	–	GND	41	O	Q3	57	–	GND
10	–	GND	26	–	V_{DD}	42	–	GND	58	–	V_{DD}
11	I	A6	27	O	R4	43	O	Q4	59	I	D0
12	I	A7	28	O	R5	44	O	Q5	60	I	D1
13	I	B0	29	O	R6	45	O	Q6	61	I	D2
14	I	B1	30	O	R7	46	O	Q7	62	I	D3
15	I	B2	31	I	MOD	47	I	C0	63	I	D4
16	I	B3	32	I	MSQ	48	I	C1	64	I	D5



INPUT

A0-A7 ; A DATA PORT
B0-B7 ; B DATA PORT
C0-C8 ; C DATA PORT
CK ; CLOCK
CLR ; CLEAR
D0-D7 ; INTERNAL REGISTER PORT
MOD ; MODE SELECT
(0:8-BIT MODE, 1:9-BIT MODE)
MSQ ; RANDOM NUMBER GENERATE
RAS ; REG A SELECT
RAW ; WRITE A REGISTER
RBS ; REG B SELECT
RBW ; WRITE B REGISTER
RND ; INTEGER DATA OUT CANCEL

OUTPUT

R0-R7 ; MINOR GROUP PORT (MSQ:0)
DUMMY RANDOM NUMBER (MSQ:1)
Q0-Q7 ; INTEGER GROUP DATA PORT