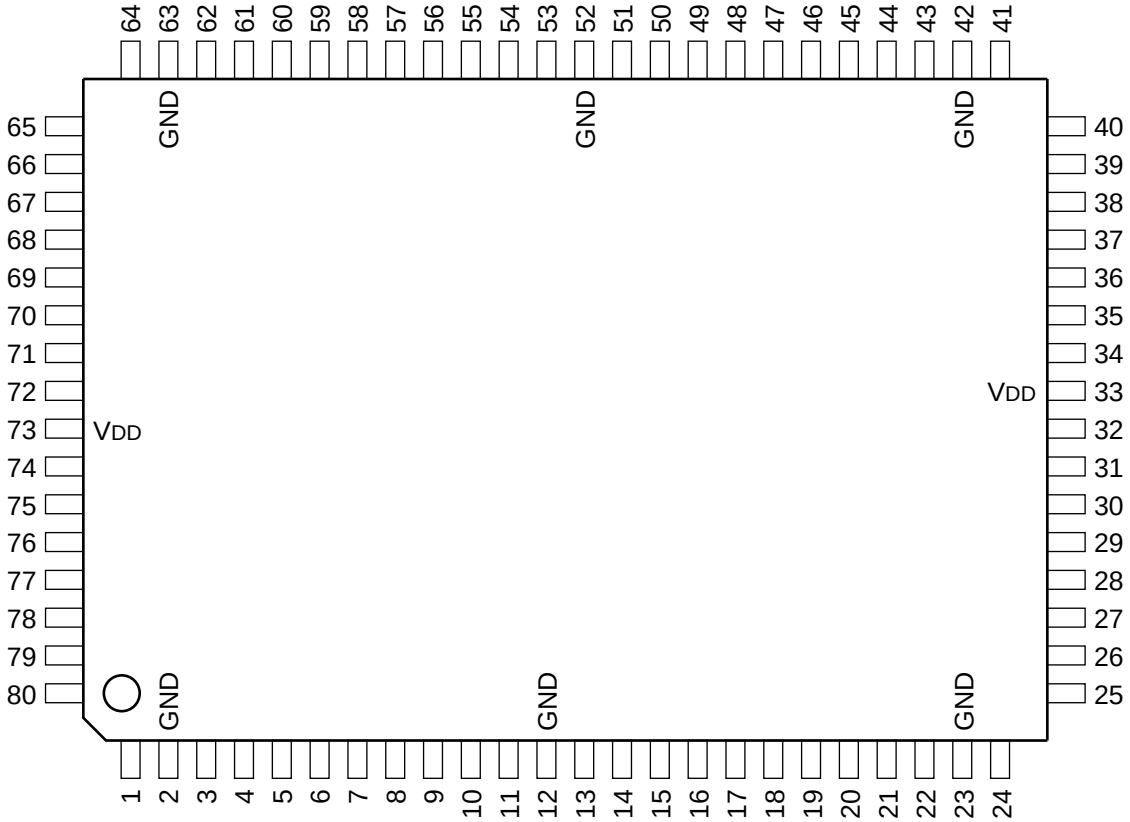
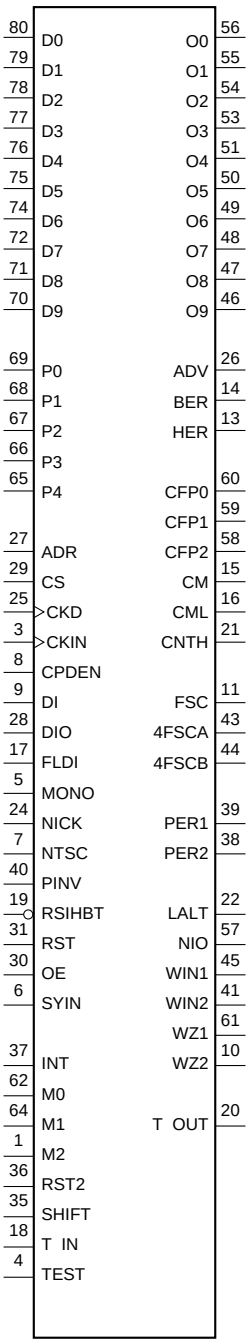
C-MOS DIGITAL CLOCK GENERATOR

— TOP VIEW —



<CPU (MASTER) MODE>

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	M2	21	O	CNTH	41	O	WIN2	61	O	WZ1
2	—	GND	22	O	LALT	42	—	GND	62	I	M0
3	I	CKIN	23	—	GND	43	O	4FSCA	63	—	GND
4	I	TEST	24	I	NICK	44	O	4FSCB	64	I	M1
5	I	MONO	25	I	CKD	45	O	WIN1	65	I	P4
6	I	SYIN	26	O	ADV	46	O	O9	66	I	P3
7	I	NTSC	27	I	ADR	47	O	O8	67	I	P2
8	I	CPDEN	28	I/O	DIO	48	O	O7	68	I	P1
9	I	DI	29	I	CS	49	O	O6	69	I	P0
10	O	WZ2	30	I	OE	50	O	O5	70	I	D9
11	O	FSC	31	I	RST	51	O	O4	71	I	D8
12	—	GND	32	—	NC	52	—	GND	72	I	D7
13	O	HER	33	—	V_{DD}	53	O	O3	73	—	V_{DD}
14	O	BER	34	—	NC	54	O	O2	74	I	D6
15	O	CM	35	I	SHIFT	55	O	O1	75	I	D5
16	O	CML	36	I	RST2	56	O	O0	76	I	D4
17	I	FLDI	37	I	INT	57	O	NIO	77	I	D3
18	I	TIN	38	O	PER2	58	O	CFP2	78	I	D2
19	I	$\overline{\text{RSIHBT}}$	39	O	PER1	59	O	CFP1	79	I	D1
20	O	TOUT	40	I	PINV	60	O	CFP0	80	I	D0



INPUT

ADR	;	SERIAL ADDRESS
CKIN	;	SYSTEM CLOCK FROM VCO (8FSC)
CKD	;	SERIAL INTERFACE CLOCK
CPDEN	;	ENABLE INPUT OF PEDESTAL CLAMP FUNCTION (OPEN OR HIGH : ENABLE)
CS	;	CHIP SELECT
D0 - D9	;	VIDEO DATA IN (MSB = D9)
DI	;	COMPOSITE/COMPONENT SELECT (HIGH : COMPONENT)
FLDI	;	CONNECT TO "CFPQ" IN THE PAL SYSTEM
INT	;	TEST PIN. (NORMAL USE IS OPEN OR HIGH)
M0 - M2	;	TEST PIN. (NORMAL USE IS OPEN OR LOW)
MONO	;	WHEN "MONO" BECOMES HIGH, THEN INTERNAL H-PLL COUNTER MAKE "WZ2" SIGNAL, AND "CM" BECOMES LOW, WHETHER "D0 - D9" INPUT HAS BURST SIGNAL OR NOT.
NICK	;	NTSC SYSTEM : CONNECT TO CNTH PAL SYSTEM : CONNECT TO "LALTO"
NTSC	;	525/625 SYSTEM SELECT (HIGH : 525)
OE	;	OUTPUT ENABLE INPUT FOR "O0 - O9"
P0 - P4	;	DELAY CONTROL FOR BURST GATE PULSE
PINV	;	POLARITY OF "PER1" AND "PER2"
$\overline{\text{RSIHBT}}$	;	RESET ENABLE FOR INTERNAL H-PLL COUNTER (LOW : ENABLE)
RST	;	RESET
RST2	;	TEST PIN. (NORMAL USE IS OPEN OR HIGH)
SHIFT	;	TEST PIN. (NORMAL USE IS OPEN OR LOW)
SYIN	;	COMPOSITE SYNC
TIN	;	TEST PIN. (NORMAL USE IS OPEN OR LOW)
TEST	;	TEST PIN. (NORMAL USE IS OPEN OR LOW)

OUTPUT

ADV	;	THIS SIGNAL SHOWS SC-H PHASE IS ADVANCE (HIGH : ADVANCE)
BER	;	BURST PHASE COMPARATOR
CFP0	;	FIELD PULSE
CFP1	;	COLOR FRAME PULSE
CFP2	;	PAL COLOR FRAME PULSE
CM	;	WHEN "MONO" IS TO HIGH, "CM" IS DERIVED TO LOW. THIS SIGNAL SHOWS BURST PRESENCE IN "D0 - D9" (HIGH : PRESENCE)
CML	;	INVERTED OUTPUT OF "CM"
CNTH	;	HORIZONTAL PULSE
FSC	;	FSC PULSE
4FSCA	;	4FSC PULSE
4FSCB	;	4FSC PULSE INVERTED
HER	;	H-PHASE COMPARATOR OUTPUT
LALT	;	LINE ALTERNATIVE PULSE OUTPUT IN THE PAL SYSTEM.
NIO	;	NI PULSE
O0 - O9	;	VIDEO DATA OUT
PER1, PER2	;	PEDESTAL DIFFERENCE COMPARATOR OUTPUT
WIN1	;	THIS SIGNAL SHOWS SC-H PHASE CENTER POSITION (HIGH : CENTER)
WIN2	;	THIS SIGNAL SHOWS SC-H PHASE IS WITHIN ± 45° (HIGH : IN)
WZ1	;	TEST OUTPUT
WZ2	;	HORIZONTAL PULSE OUTPUT WHICH IS SYNCHRONIZED BY FSC
TOUT	;	TEST OUTPUT

INPUT/OUTPUT

DIO	;	SERIAL DATA

CONTROL METHODS

1. I/O ADDRESS MAP

ADDRESS	FUNCTION
0	WRITE ZERO PHASE (COLOR)
1	WRITE ZERO PHASE (MONO)
2	SC-H PHASE ADJUST
3	SAMPLING PHASE (sin θs)
4	SAMPLING PHASE (sin < θs + π/4 >)
5	PEDESTAL CLAMP VALUE
6	FORCED MONO MODE

2. DETAIL OF FUNCTION

(A) ADDRESS = 0

DATA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

PHASE (D15 = MSB)

1LSB = 1 CLOCK WIDTH (CLOCK = 4FSC)

PHASE RANGE
- NTSC ··· 0 - 909
- PAL ··· 0 - 1134
- D1 525 ··· 0 - 857
- D1 625 ··· 0 - 863

(B) ADDRESS = 1

DATA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												x	x	x	x

PHASE (D15 = MSB)

1LSB = 1/2 CLOCK WIDTH
(CLOCK = nF_H : n IS DESIDED BY SYSTEM)

n
- NTSC ··· 910
- PAL ··· 1135
- D1 525 ··· 858
- D1 625 ··· 864

(C) ADDRESS = 2

DATA

D7	D6	D5	D4	D3	D2	D1	D0

SC-H PHASE

1LSB ≒ 1/64 CLOCK WIDTH

(D) ADDRESS = 3 OR 4 (SET BOTH sin θs AND sin θs + π/4)

DATA

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

PHASE (D9 = MSB)

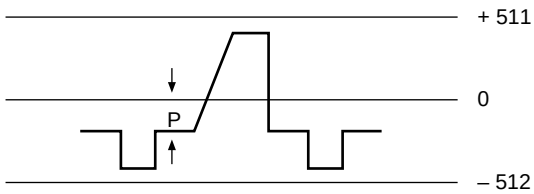
PHASE = 511 *sin θs (2's COMPLEMENT)

(E) ADDRESS = 5

DATA

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

PEDESTAL (D9 = MSB)



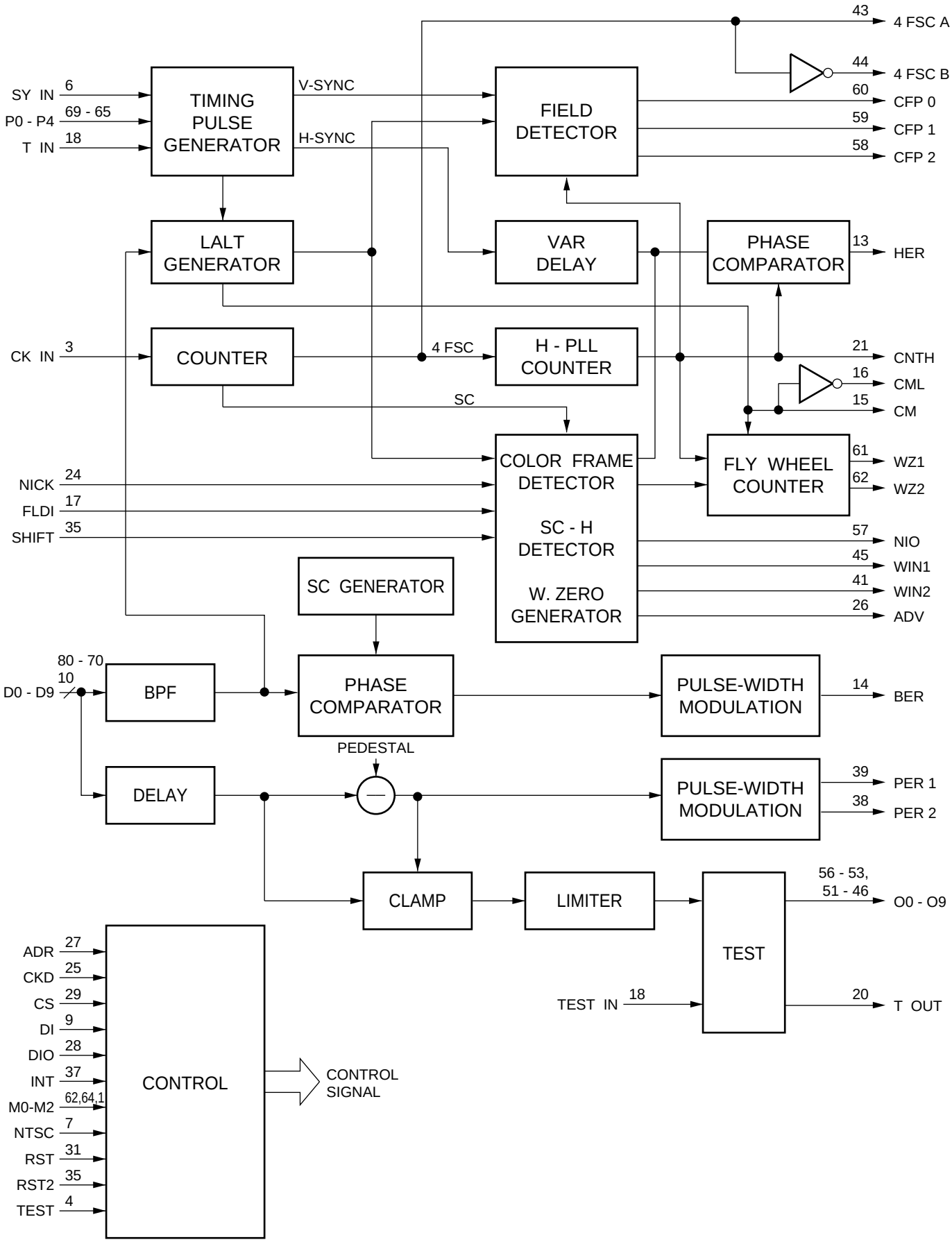
P = 272 (NTSC)

(2's COMPLEMENT)

(F) ADDRESS = 6

D0

H : FORCED MONO MODE
L : AUTO (DECIDED BY BURST PRESENCE OF INPUT)


SY IN
6
P0 - P4
69 - 65
T IN
18
TIMING PULSE GENERATOR
V-SYNC
H-SYNC
FIELD DETECTOR
43
4 FSC A
44
4 FSC B
60
CFP 0
59
CFP 1
58
CFP 2
LALT GENERATOR
VAR DELAY
PHASE COMPARATOR
13
HER
CK IN
3
COUNTER
4 FSC
H - PLL COUNTER
21
CNTH
16
CML
15
CM
SC
COLOR FRAME DETECTOR
SC - H DETECTOR
W. ZERO GENERATOR
FLY WHEEL COUNTER
61
WZ1
62
WZ2
NICK
24
FLDI
17
SHIFT
35
57
NIO
45
WIN1
41
WIN2
26
ADV
SC GENERATOR
80 - 70
10
D0 - D9
BPF
PHASE COMPARATOR
PULSE-WIDTH MODULATION
14
BER
PEDESTAL
DELAY
PULSE-WIDTH MODULATION
39
PER 1
38
PER 2
CLAMP
LIMITER
TEST
56 - 53,
51 - 46
O0 - O9
TEST IN
18
20
T OUT
ADR
27
CKD
25
CS
29
DI
9
DIO
28
INT
37
M0-M2
62,64,1
NTSC
7
RST
31
RST2
35
TEST
4
CONTROL
CONTROL SIGNAL