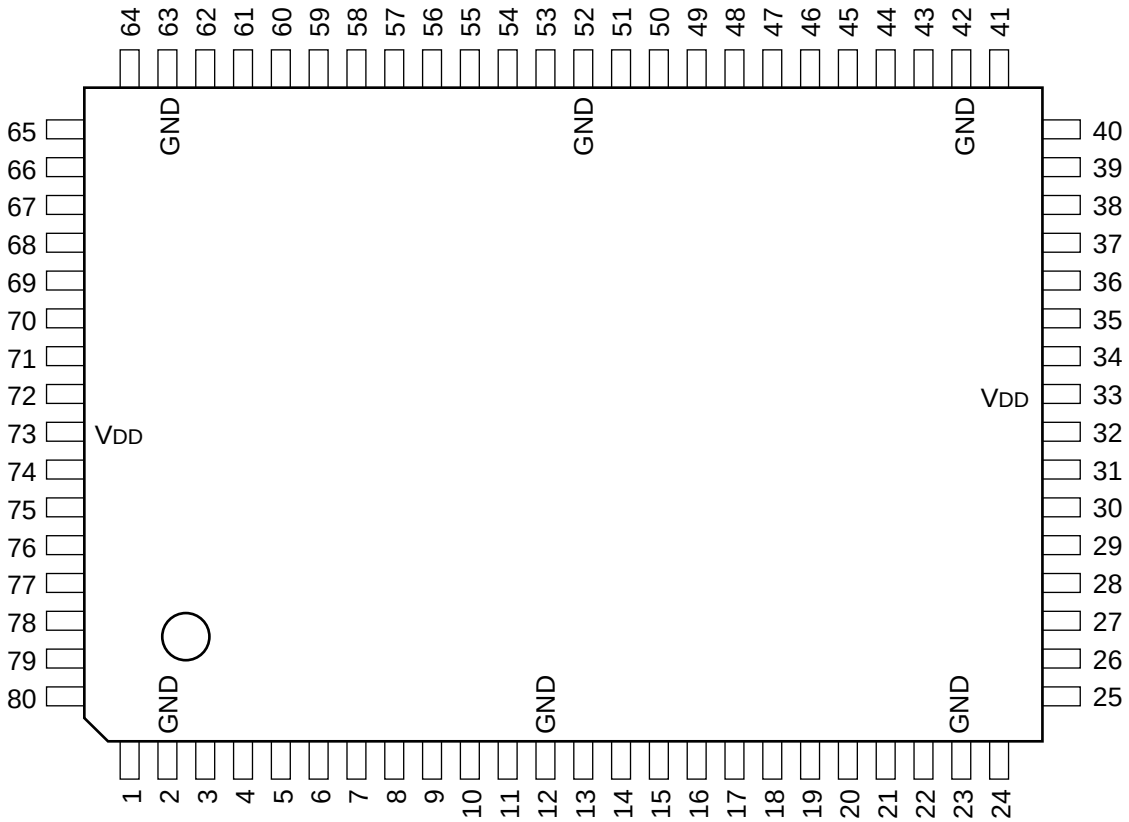
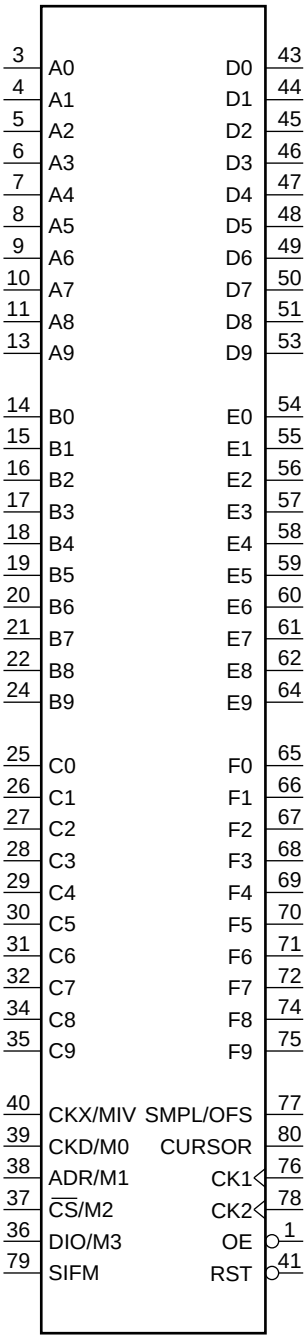
C-MOS SUPER MULTIPLEX-DEMULTIPLEXER

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	$\overline{OE}$	21	I/O	B7	41	I	$\overline{RST}$	61	I/O	E7
2	—	GND	22	I/O	B8	42	—	GND	62	I/O	E8
3	I/O	A0	23	—	GND	43	I/O	D0	63	—	GND
4	I/O	A1	24	I/O	B9	44	I/O	D1	64	I/O	E9
5	I/O	A2	25	I/O	C0	45	I/O	D2	65	I/O	F0
6	I/O	A3	26	I/O	C1	46	I/O	D3	66	I/O	F1
7	I/O	A4	27	I/O	C2	47	I/O	D4	67	I/O	F2
8	I/O	A5	28	I/O	C3	48	I/O	D5	68	I/O	F3
9	I/O	A6	29	I	C4	49	I/O	D6	69	I	F4
10	I/O	A7	30	I	C5	50	I/O	D7	70	I	F5
11	I/O	A8	31	I	C6	51	I/O	D8	71	I	F6
12	—	GND	32	I	C7	52	—	GND	72	I	F7
13	I/O	A9	33	—	V_{DD}	53	I/O	D9	73	—	V_{DD}
14	I/O	B0	34	I	C8	54	I/O	E0	74	I	F8
15	I/O	B1	35	I	C9	55	I/O	E1	75	I	F9
16	I/O	B2	36	I/O	DIO/M3	56	I/O	E2	76	I	CK1
17	I/O	B3	37	I	$\overline{CS}$/M2	57	I/O	E3	77	I	SMPL/OFS
18	I/O	B4	38	I	ADR/M1	58	I/O	E4	78	I	CK2
19	I/O	B5	39	I	CKD/M0	59	I/O	E5	79	I	SIFM
20	I/O	B6	40	I	CKX/MIV	60	I/O	E6	80	I	CURSOR



COMMON TERMINALS

A0 - A9	; CHA 10-BIT DIGITAL INPUT/OUTPUT
B0 - B9	; CHB 10-BIT DIGITAL INPUT/OUTPUT
C0 - C9	; CHC 10-BIT DIGITAL INPUT/OUTPUT
CK1	; SYSTEM CLOCK INPUT
CK2	; SUB-CLOCK INPUT
CURSOR	; CURSOR INPUT
D0 - D9	; CHD 10-BIT DIGITAL INPUT/OUTPUT
E0 - E9	; CHE 10-BIT DIGITAL INPUT/OUTPUT
F0 - F9	; CHF 10-BIT DIGITAL INPUT/OUTPUT
$\overline{OE}$	; OUTPUT ENABLE INPUT (LOW : ENABLE)
$\overline{RST}$	; RESET PULSE INPUT (LOW : RESET)
SIFM	; SERIAL INTERFACE MODE (SIF)/ MANUAL MODE SELECT INPUT (LOW : SERIAL INTERFACE MODE, HIGH : MANUAL MODE)

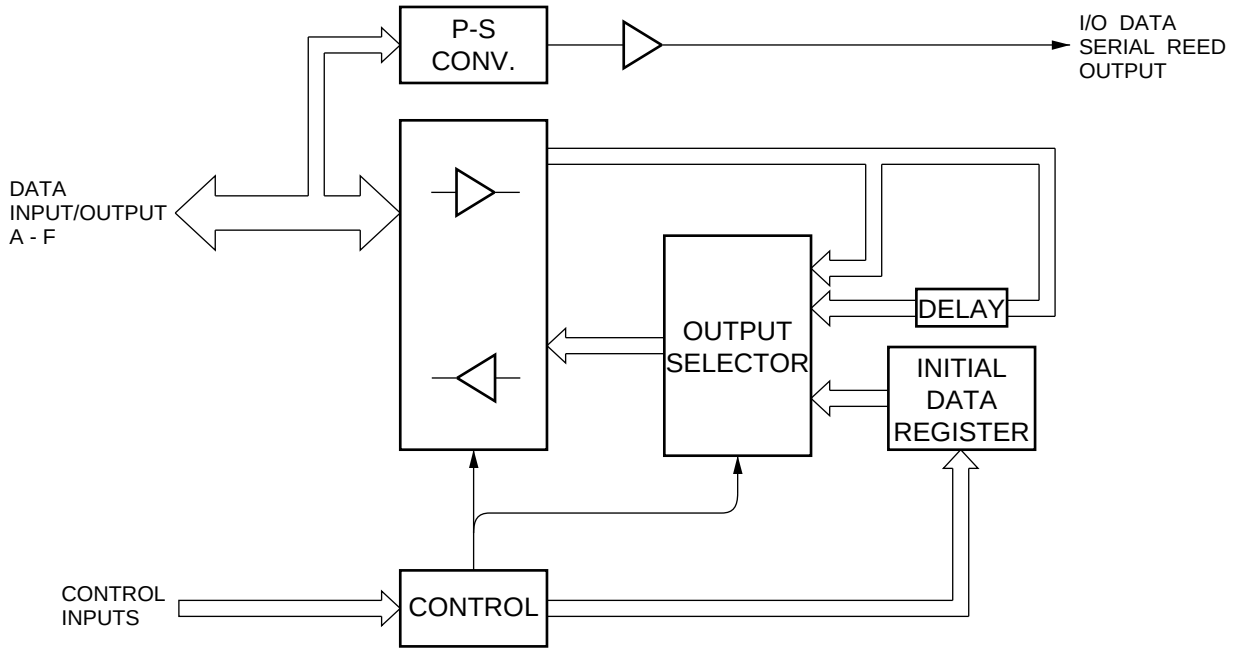
TERMINALS OF MANUAL MODE

M0 - M3	; MODE SELECT INPUT (4-BIT)
MIV	; MSB INVERT CONTROL INPUT (HIGH : INVERT MSB)
OFS	; CURSOR MSB INVERT CONTROL INPUT

TERMINALS OF SIF MODE

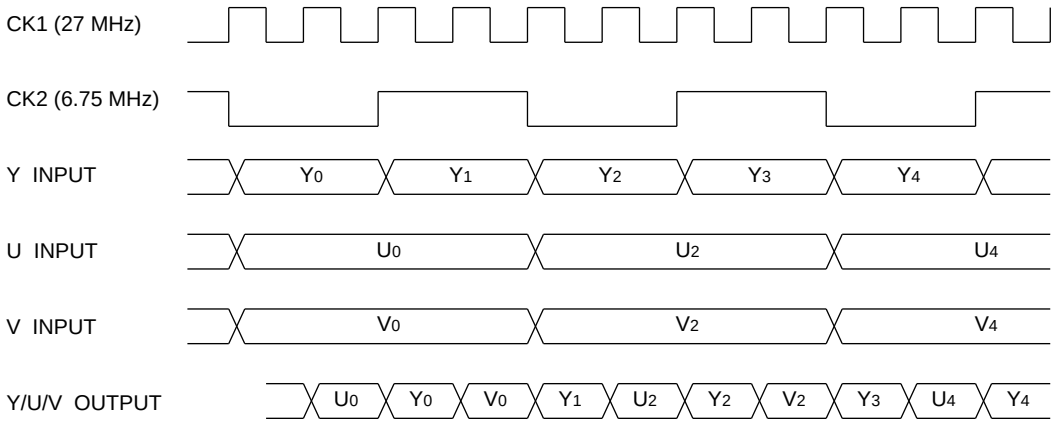
ADR	; SERIAL ADDRESS INPUT
CKD	; SERIAL INTERFACE CLOCK INPUT
CKX	; SWITCHING TIMING PULSE INPUT
$\overline{CS}$	; CHIP SELECT INPUT (LOW: ACTIVE)
DIO	; SERIAL DATA INPUT/OUTPUT
SMPL	; SAMPLING PULSE INPUT

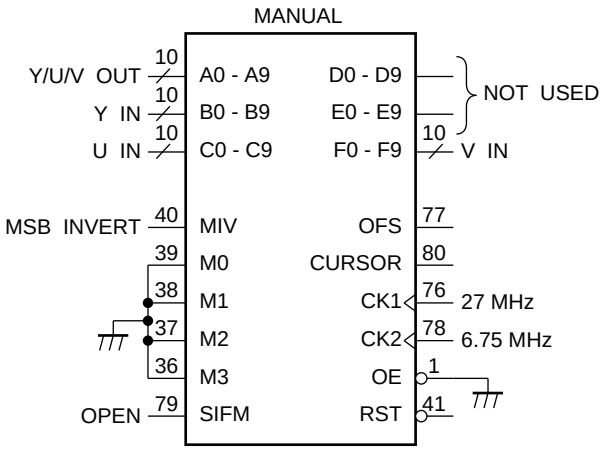
BLOCK DIAGRAM

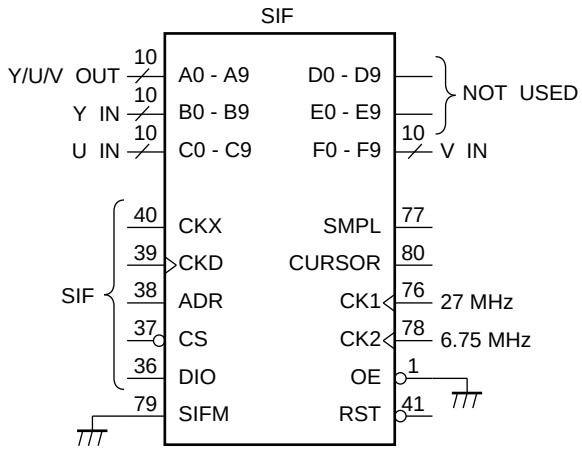


FUNCTION OF MODE 0-MODE 12

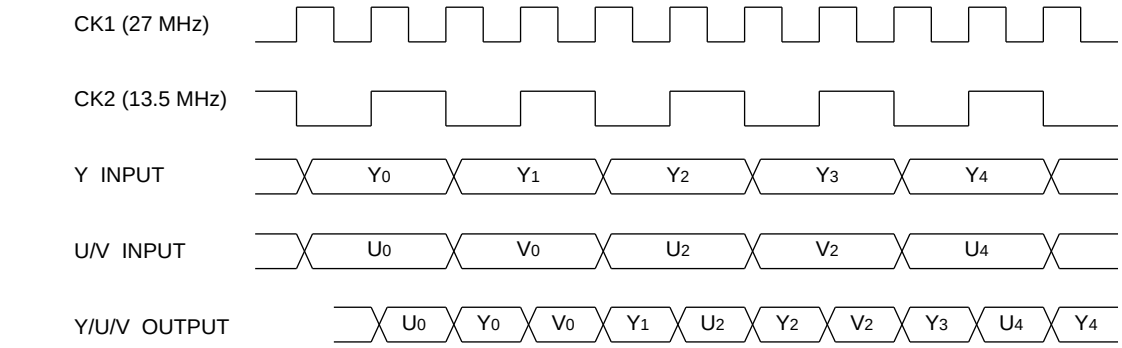
MODE 0: D1 Y, U, V MULTIPLEXER

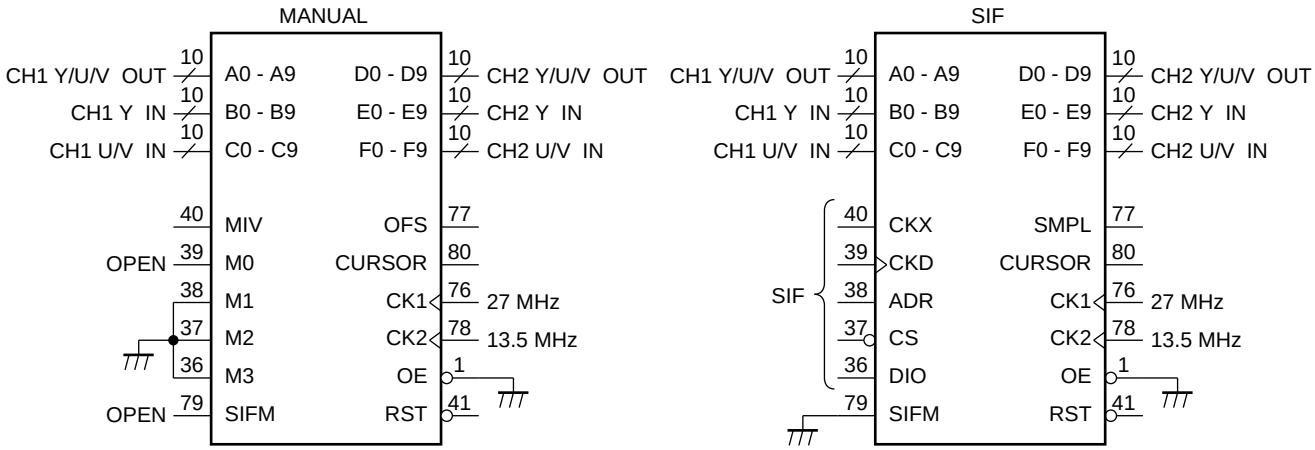




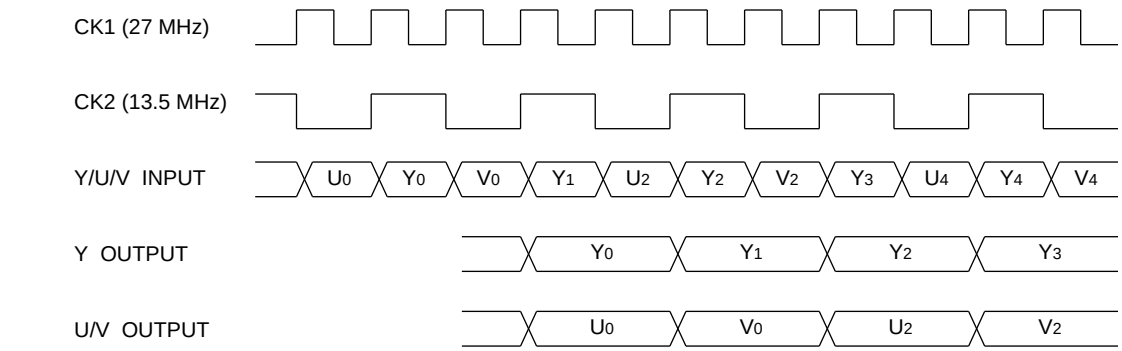


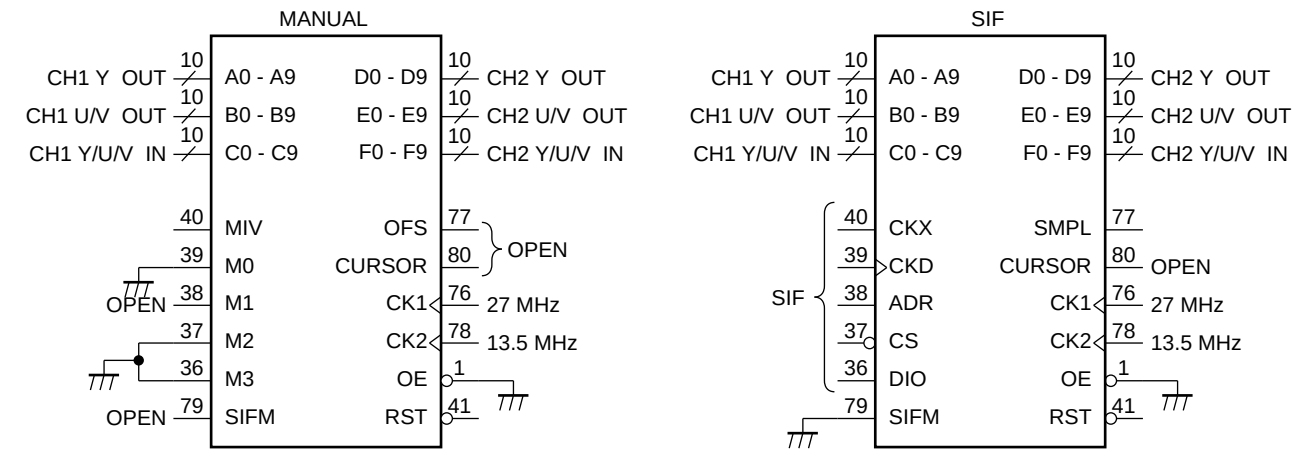
MODE 1: D1 Y, U/V MULTIPLEXER (2CH)



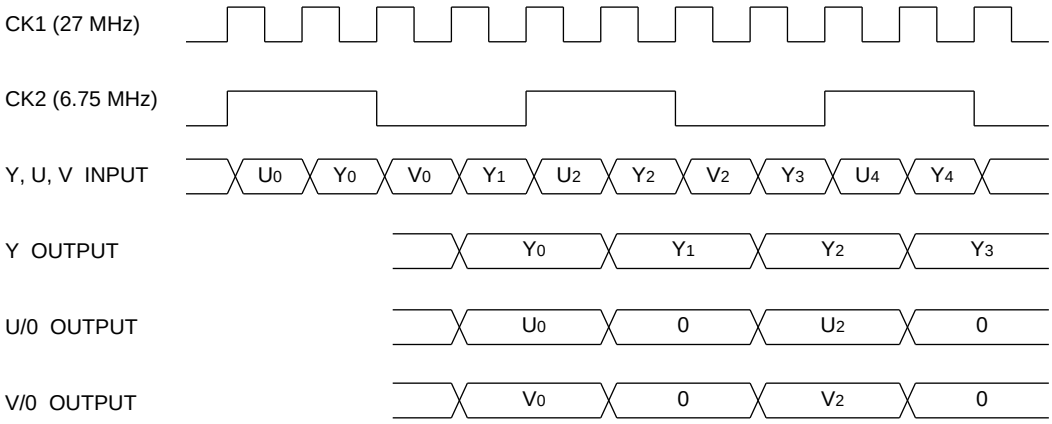


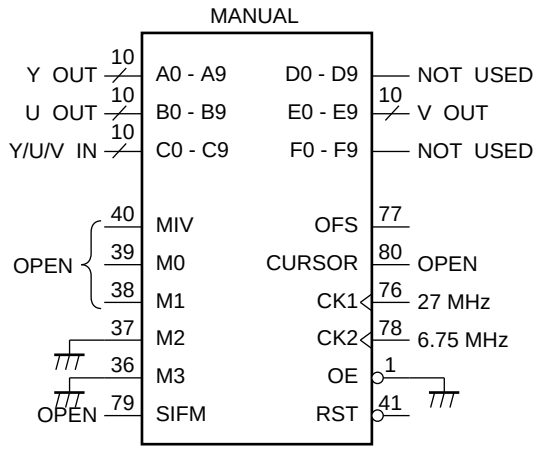
MODE 2 : D1 Y, U/V DEMULTIPLEXER (2CH)

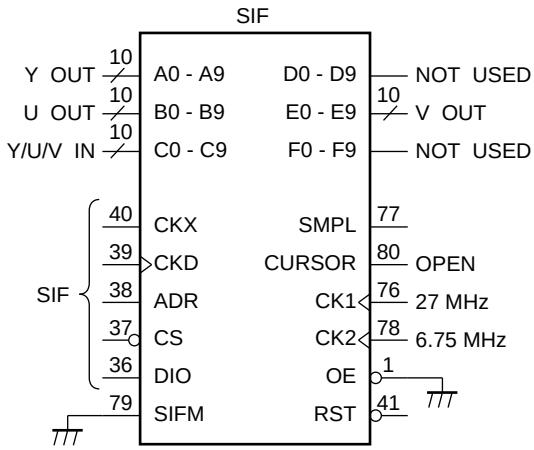




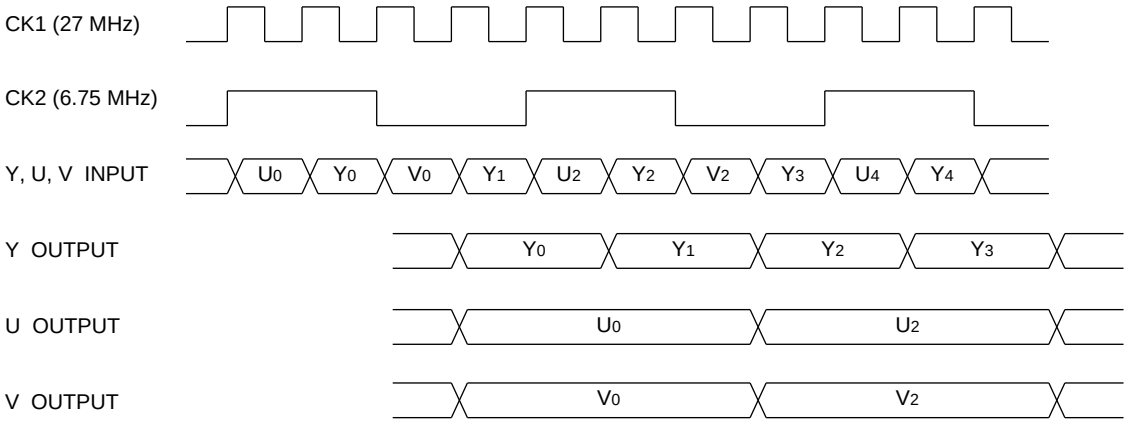
MODE 3 : D1 Y, U, V DEMULTIPLEXER (WITH 0 INSERT FUNCTION)

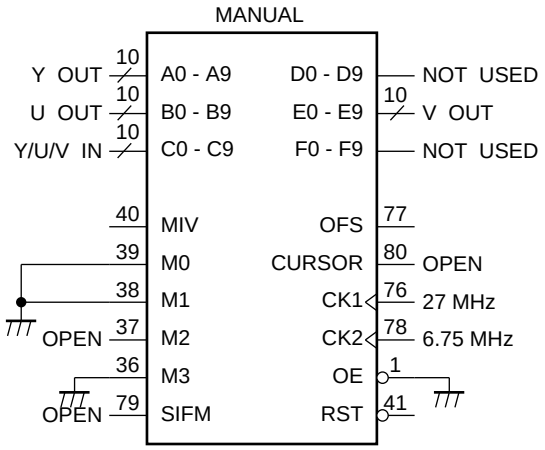


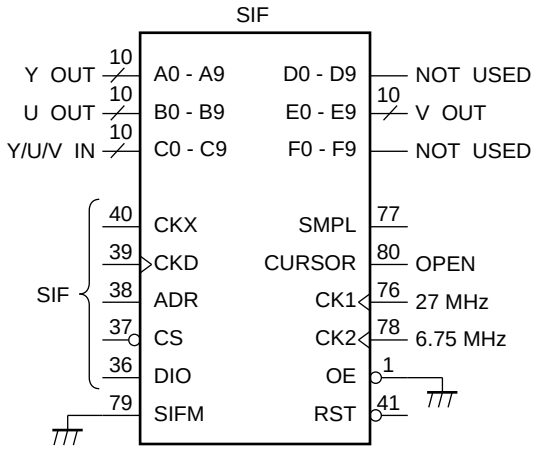




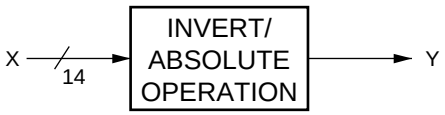
MODE 4 : D1 Y, U, V DEMULTIPLEXER





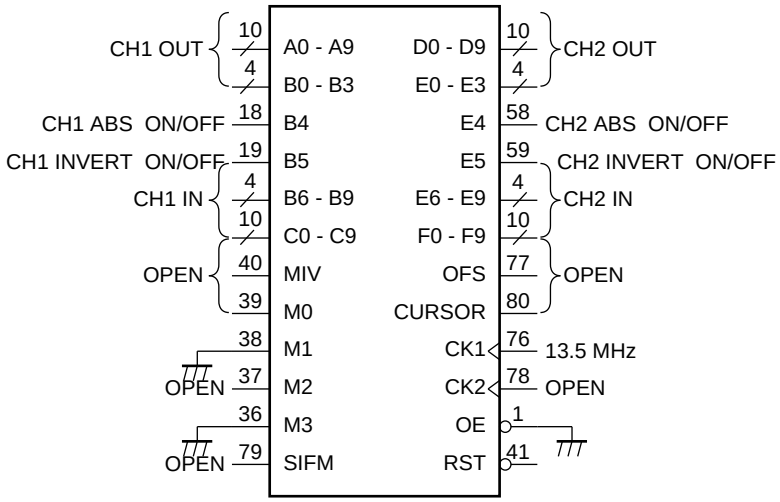


MODE 5 : ABSOLUTE OR INVERT VALUE OPERATION (2CH)

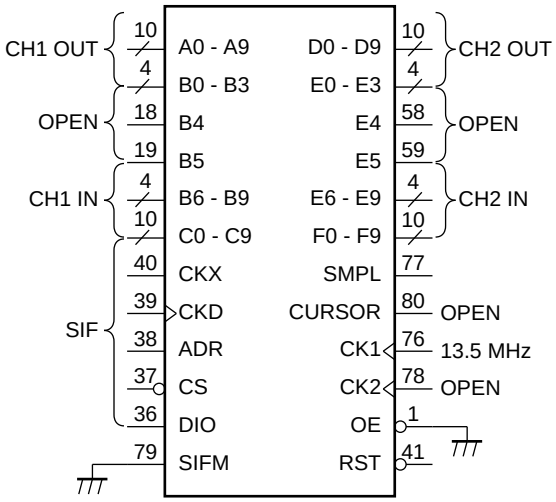


$Y = X \text{ OR } \overline{X} \text{ OR } |X| \text{ OR } |\overline{X}|$

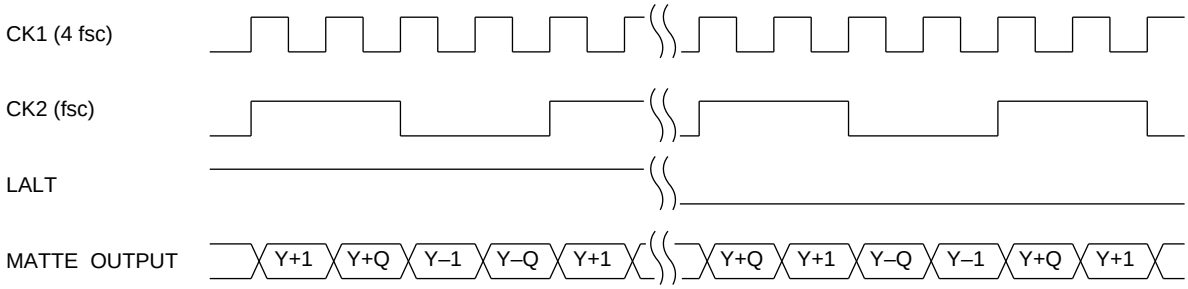
MANUAL

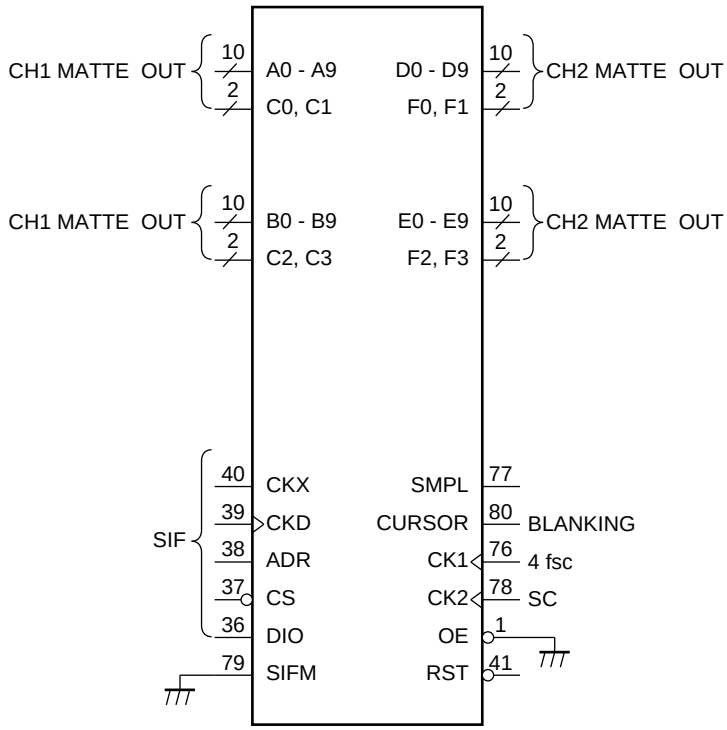


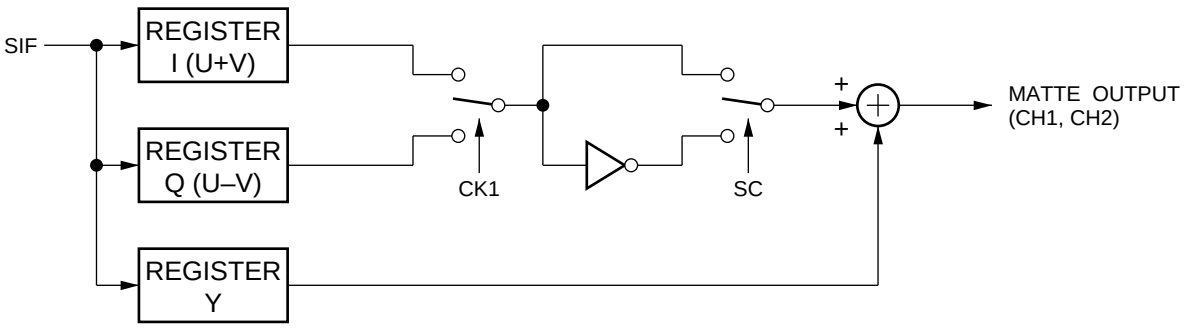
SIF



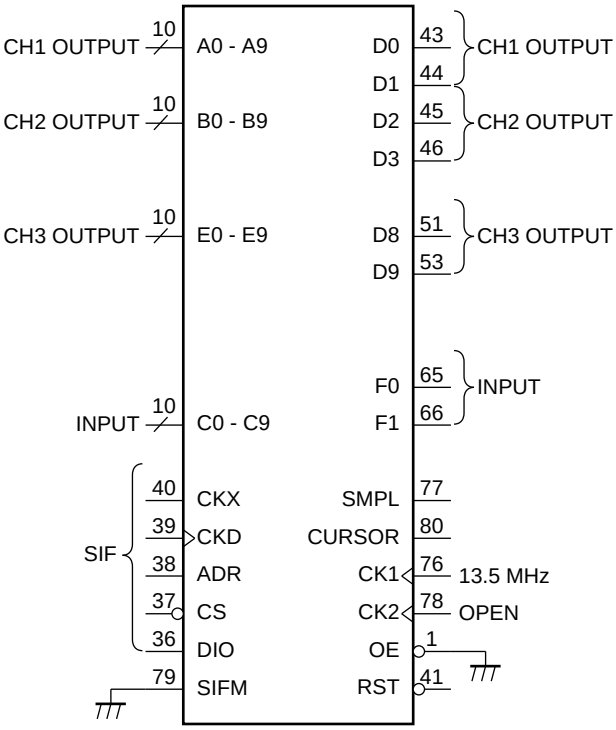
MODE 6 : D2 MATTE GENERATOR (2CH)

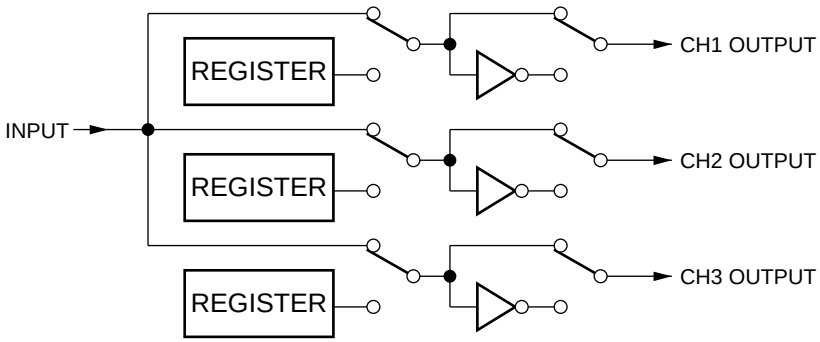




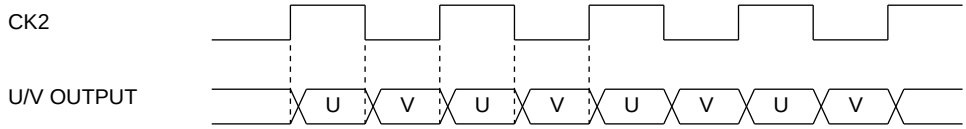


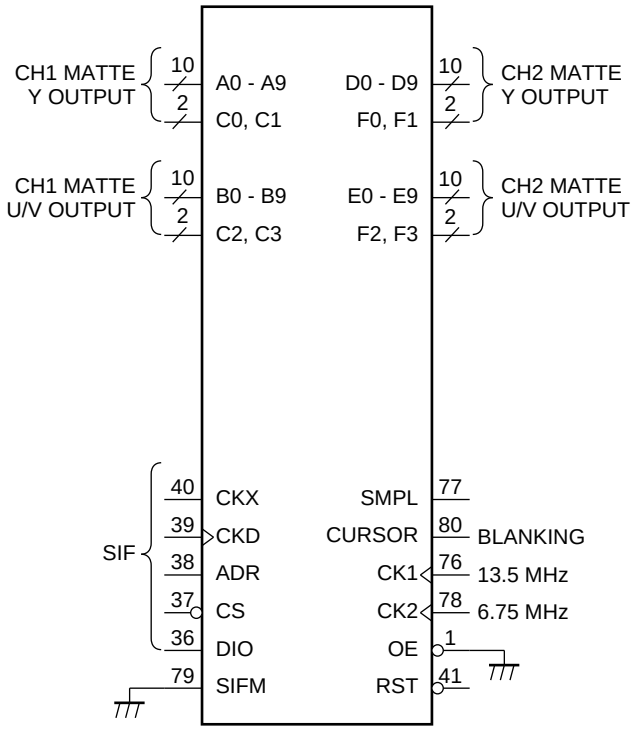
MODE 7 : WIPE/MIX TRANSITION CONTROLLER (3CH OUTPUTS)

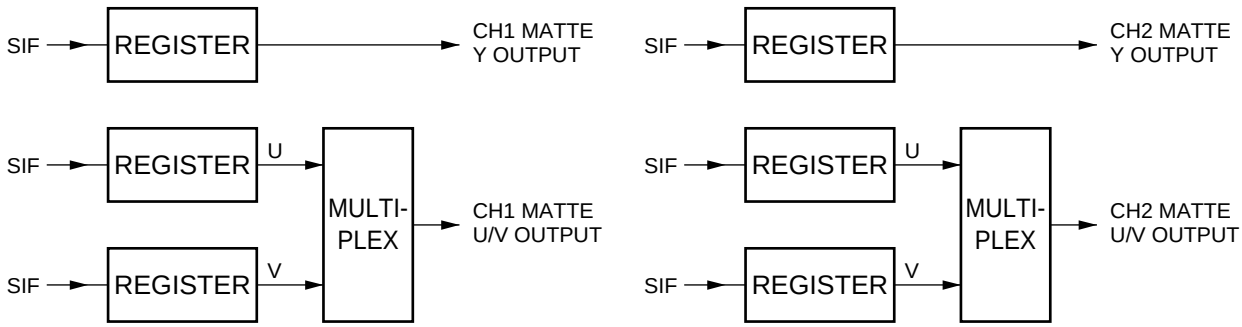




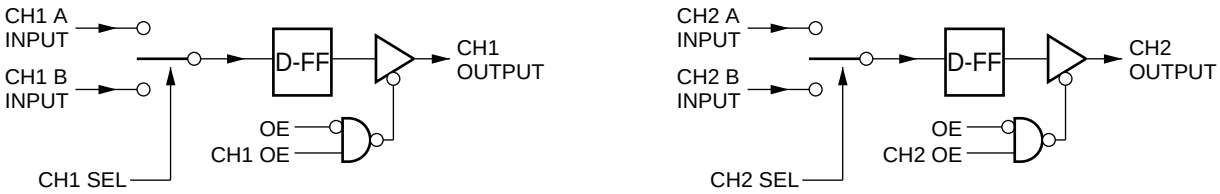
MODE 8 : D1 MATTE GENERATOR (2CH)

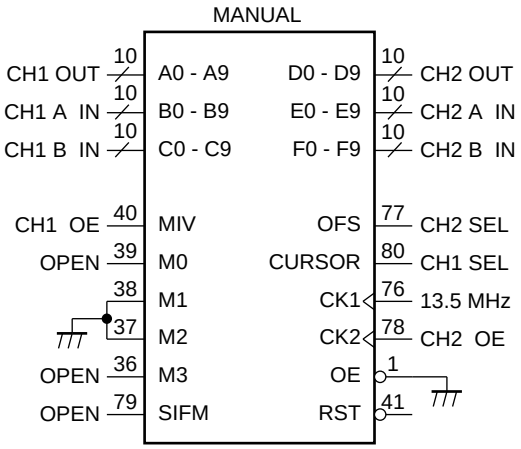




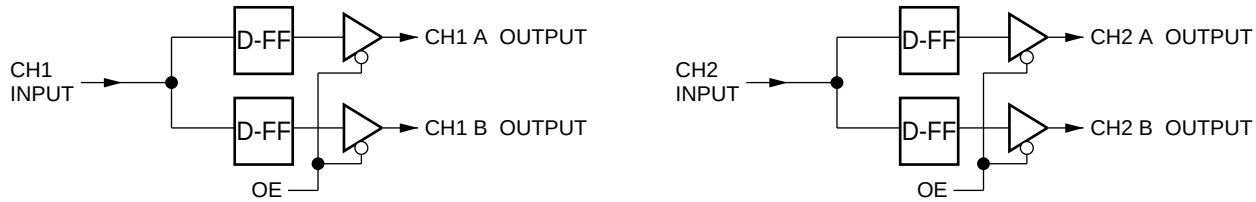


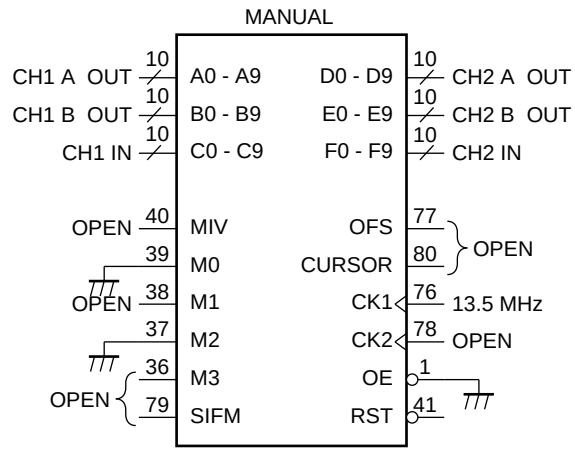
MODE 9 : 1 OF 2 SELECTOR (2CH)



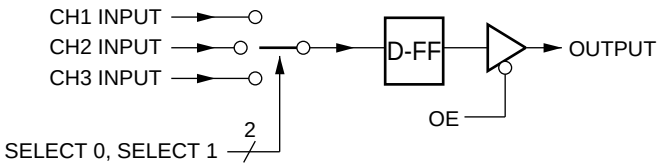


MODE 10 : 1 TO 2 DISTRIBUTER (2CH)



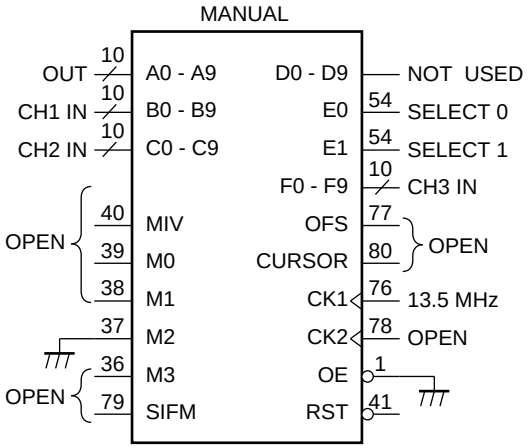


MODE 11 : 1 OF 3 SELECTOR



SELECT 1	SELECT 0	OUTPUT
0	0	CH1
0	1	CH2
1	0	CH3
1	1	0 OUT

0 ; LOW LEVEL
1 ; HIGH LEVEL



MODE 12 : 1 TO 3 DISTRIBUTER