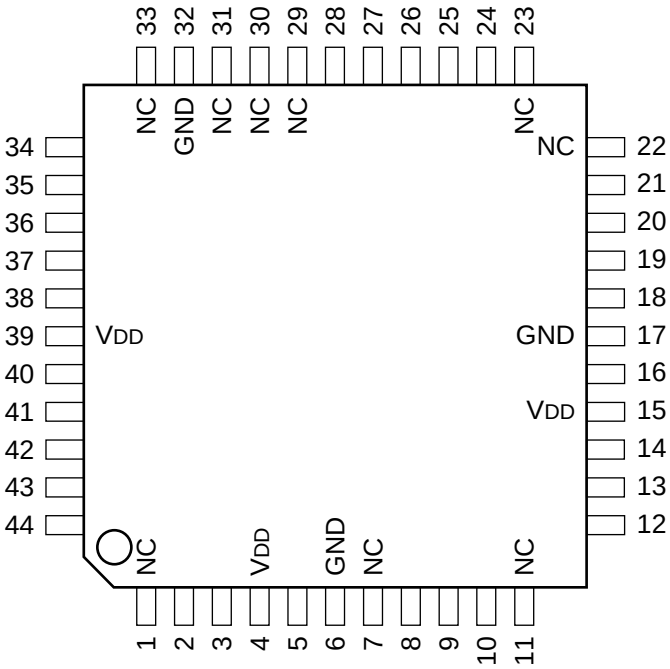
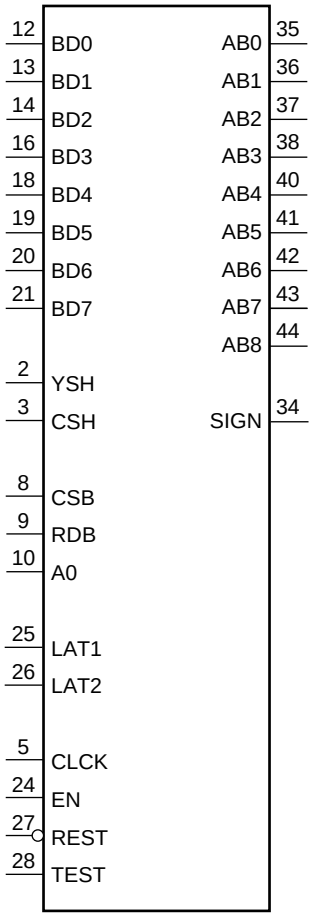
DT Y/C DELAY DETECTOR

—TOP VIEW—





PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	23	—	NC
2	I	YSH	24	I	EN
3	I	CSH	25	I	LAT1
4	—	V_{DD}	26	I	LAT2
5	I	CLCK	27	I	$\overline{\text{REST}}$
6	—	GND	28	I	TEST
7	—	NC	29	—	NC
8	I	CSB	30	—	NC
9	I	RDB	31	—	NC
10	I	A0	32	—	GND
11	—	NC	33	—	NC
12	I	BD0	34	O	SIGN
13	I	BD1	35	O	AB0
14	I	BD2	36	O	AB1
15	—	V_{DD}	37	O	AB2
16	I	BD3	38	O	AB3
17	—	GND	39	—	V_{DD}
18	I	BD4	40	O	AB4
19	I	BD5	41	O	AB5
20	I	BD6	42	O	AB6
21	I	BD7	43	O	AB7
22	—	NC	44	O	AB8

INPUT

A0 : DT
BD0 - BD7 : BIT DATA
CLCK : CLOCK
CSB : DT CS
CSH : C SAMPLING HOLD
EN : ENABLE
LAT1, LAT2 : LATCH1, 2
RDB : DT RD
$\overline{\text{REST}}$: RESET
TEST : TEST
YSH : Y SAMPLING HOLD

OUTPUT

AB0 - AB8 : BIT DATA
SIGN : SIGN