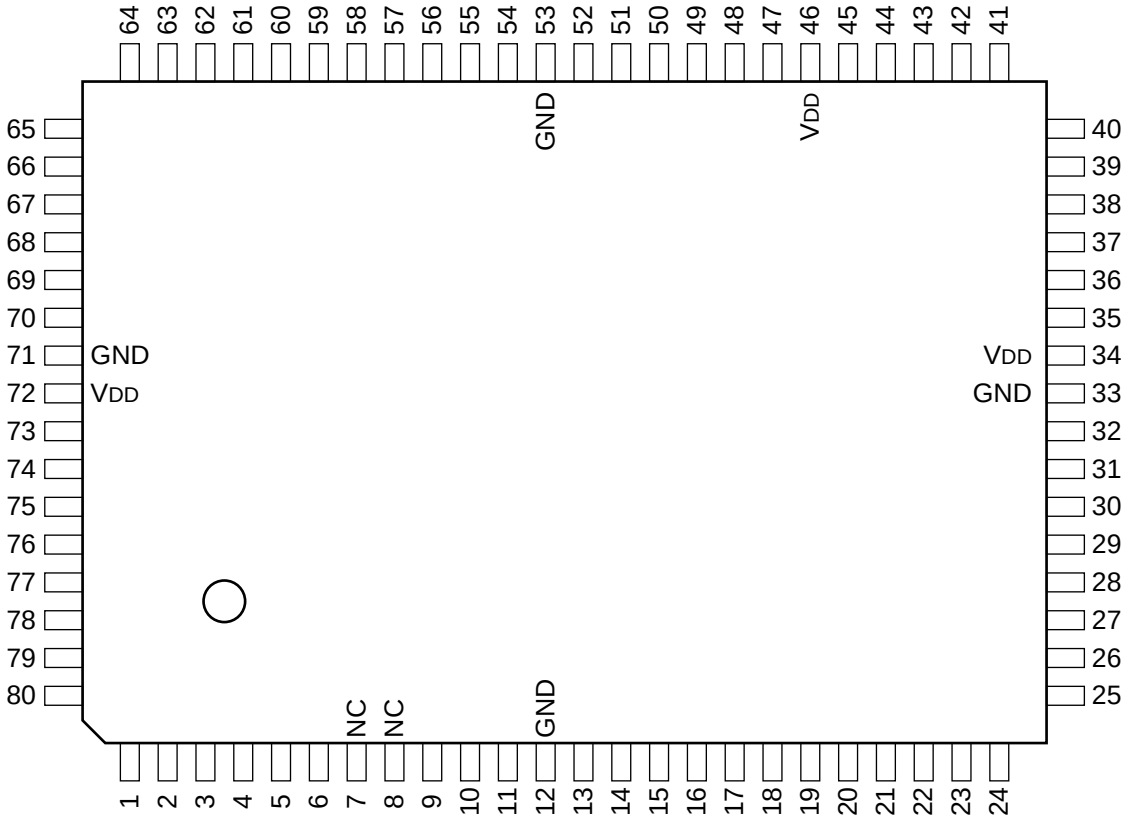
C-MOS DUAL PORT RAM CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	DOL	21	I/O	D7R	41	I/O	D6M	61	I	A10L
2	I	$\overline{\text{WRL}}$	22	I/O	D6R	42	I/O	D5M	62	I	A9L
3	I	$\overline{\text{RDL}}$	23	I/O	D5R	43	I/O	D4M	63	I	A8L
4	O	$\overline{\text{WAITL}}$	24	I/O	D4R	44	I/O	D3M	64	I	A7L
5	I	$\overline{\text{CSL}}$	25	I/O	D3R	45	I/O	D2M	65	I	A6L
6	I	$\overline{\text{CKL}}$	26	I/O	D2R	46	—	VDD	66	I	A5L
7	—	NC	27	I/O	D1R	47	I/O	D1M	67	I	A4L
8	—	NC	28	I/O	D0R	48	I/O	D0M	68	I	A3L
9	I	A10R	29	I	$\overline{\text{WRR}}$	49	O	A0M	69	I	A2L
10	I	A9R	30	I	$\overline{\text{RDR}}$	50	O	A1M	70	I	A1L
11	I	A8R	31	O	$\overline{\text{WAITR}}$	51	O	A2M	71	—	GND
12	—	GND	32	I	$\overline{\text{CSR}}$	52	O	A3M	72	—	VDD
13	I	A7R	33	—	GND	53	—	GND	73	I	A0L
14	I	A6R	34	—	VDD	54	O	A4M	74	I/O	D7L
15	I	A5R	35	I	CKR	55	O	A5M	75	I/O	D6L
16	I	A4R	36	I	CKT	56	O	A6M	76	I/O	D5L
17	I	A3R	37	O	$\overline{\text{WEM}}$	57	O	A7M	77	I/O	D4L
18	I	A2R	38	O	$\overline{\text{OEM}}$	58	O	A8M	78	I/O	D3L
19	I	A1R	39	O	$\overline{\text{CEM}}$	59	O	A9M	79	I/O	D2L
20	I	A0R	40	I/O	D7M	60	O	A10M	80	I/O	D1L

INPUT

A0L - A10L	;	ADDRESS BUS OF PORT L
A0R - A10R	;	ADDRESS BUS OF PORT R
CKL	;	CLOCK OF PORT L
CKR	;	CLOCK OF PORT R
CKT	;	CLOCK
CSL	;	CHIP SELECT OF PORT L
CSR	;	CHIP SELECT OF PORT R
RDL	;	READ STROBE OF PORT L
RDR	;	READ STROBE OF PORT R
WRL	;	WRITE STROBE OF PORT L
WRR	;	WRITE STROBE OF PORT R

OUTPUT

A0M - A10M	;	ADDRESS BUS FOR MEMORY DEVICE
CEM	;	CHIP ENABLE FOR MEMORY DEVICE
OEM	;	OUTPUT ENABLE FOR MEMORY DEVICE
WAITL	;	WAIT OF PORT L
WAITR	;	WAIT OF PORT R
WEM	;	WRITE ENABLE FOR MEMORY DEVICE

INPUT/OUTPUT

D0L - D7L	;	DATA BUS OF PORT L
D0M - D7M	;	DATA BUS FOR MEMORY DEVICE
D0R - D7R	;	DATA BUS OF PORT R