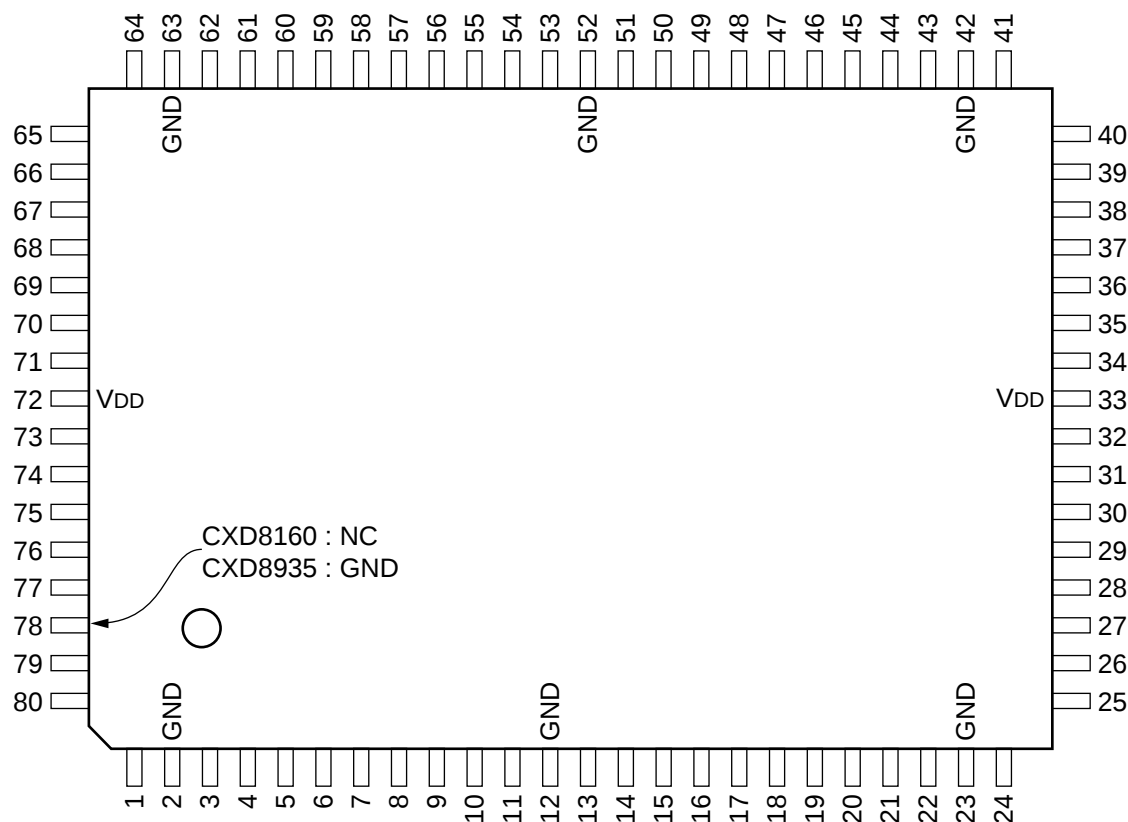


C-MOS CHROMA LINE CRAWL CANCELLER AND DIGITAL CLAMPER

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	TLOAD	21	I	$\overline{DT}$	41	O	RY1	61	O	BY6
2	—	GND	22	I	TRST	42	—	GND	62	O	BY7
3	I	CK	23	—	GND	43	O	RY2	63	—	GND
4	I	$\overline{BID}$	24	I	CIN0	44	O	RY3	64	O	BY8
5	I	$\overline{CBLK}$	25	I	CIN1	45	O	RY4	65	O	BY9
6	I	$\overline{VBLK}$	26	I	CIN2	46	O	RY5	66	I	$\overline{ENBY}$
7	I	BY	27	I	CIN3	47	O	RY6	67	I	HSYNC
8	I	XTRE	28	I	CIN4	48	O	RY7	68	I	DTSTB
9	I	XTWE	29	I	CIN5	49	O	RY8	69	I	SLD
10	O	TRO0	30	I	CIN6	50	O	RY9	70	O	SOUT
11	O	TRO1	31	I	CIN7	51	I	$\overline{ENRY}$	71	I	SDATA
12	—	GND	32	I	CIN8	52	—	GND	72	I	SCK
13	I	$\overline{FRCOMB}$	33	—	VDD	53	I	TRI0	73	—	VDD
14	I	$\overline{COMB OFF}$	34	I	CIN9	54	I	XMM	74	I	XTST0
15	I	$\overline{625}$	35	I	TRI1	55	O	BY0	75	I	XTST1
16	I	$\overline{C MUTE 1}$	36	I	TRI2	56	O	BY1	76	I	XTST2
17	I	$\overline{C MUTE 2}$	37	I	TRI3	57	O	BY2	77	I	XTST3
18	I	$\overline{CMPLX}$	38	I	TRI4	58	O	BY3	78	—	NC (CXD8160) GND (CXD8935)
19	I	$\overline{3S4}$	39	I	TRI5	59	O	BY4	79	O	ENS0
20	I	$\overline{AP OFF}$	40	O	RY0	60	O	BY5	80	O	ENS1

24	CIN0	PY0	40
25	CIN1	PY1	41
26	CIN2	PY2	43
27	CIN3	PY3	44
28	CIN4	PY4	45
29	CIN5	PY5	46
30	CIN6	PY6	47
31	CIN7	PY7	48
32	CIN8	RY8	49
34	CIN9	RY9	50
3	CK	BY0	55
5	CBLK	BY1	56
6	VBLK	BY2	57
7	BY	BY3	58
13	FRCOMB	BY4	59
14	COMB OFF	BY5	60
15	625	BY6	61
18	CMPLX	BY7	62
19	3S4	BY8	64
20	AP OFF	BY9	65
16	C MUTE1		
17	C MUTE2	ENS0	79
51	ENRY	ENS1	80
66	ENBY		
67	HSYNC		
68	DTSTB		
4	BID		
21	DT		
71	SDATA		
72	SCK	SOUT	70
69	SLD		
53	TRI0		
35	TRI1	TRO0	10
36	TRI2	TRO1	11
37	TRI3		
38	TRI4		
39	TRI5		
74	XTST0		
75	XTST1		
76	XTST3		
77	XTST4		
8	XTRE		
9	XTWE		
1	TLOAD		
54	XMM		

INPUT

3S4	; L : COMPRESS BY 3/4
625	; LIMITER LEVEL (H : 12.5%, L : 6.25%)
AP OFF	; L : SIN (X)/X CORRECTION OFF
BID	; L : BIDIREX
BY	; COMPLEXED CHROMA DATA POSITION (H : R-Y, L : B-Y)
CBLK	; L : COMPOSITE BLANKING
CIN0 - CIN9	; COMPLEXED CHROMA DATA (10-BIT)
CK	; SYSTEM CLOCK
CMPLX	; L : COMPLEX
C MUTE1, 2	; L : CHROMA DATA MUTE
COMB OFF	; L : COMB FILTER OFF MODE
DT	; L : DYNAMIC TRACKING MODE
DTSTB	; TEST MODE B-Y/R-Y STROBE
ENBY	; L : B-Y ENABLE
ENRY	; L : R-Y ENABLE
FRCOMB	; L : COMB FILTER ON MODE
HSYNC	; HORIZONTAL SYNC
SCK	; SERIAL CLOCK
SDATA	; SERIAL DATA
SLD	; SERIAL LATCH PULSE
TLOAD	; TEST MODE
TRI0 - TRI5	; TEST MODE
TRST, XMM	; TEST MODE
VBLK	; L : V BLANKING
XTRE	; TEST MODE
XTST0 - 3	; TEST MODE
XTWE	; TEST MODE

OUTPUT

BY0-BY9	; B-Y CHROMA DATA or COMPLEXED CHROMA DATA
ENS0, 1	; COMPRESS CHROMA EDGE DATA
RY0 - RY9	; R-Y CHROMA DATA or COMPLEXED DATA for D1 INTERFACE
SOUT	; SERIAL DATA
TRO0, 1	; TEST MODE