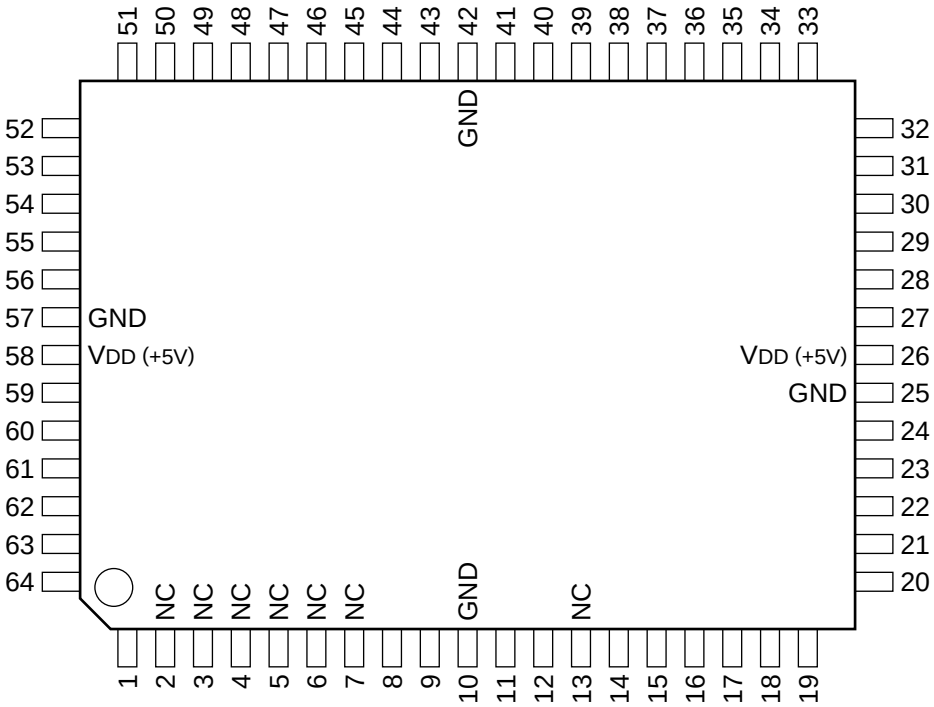
****

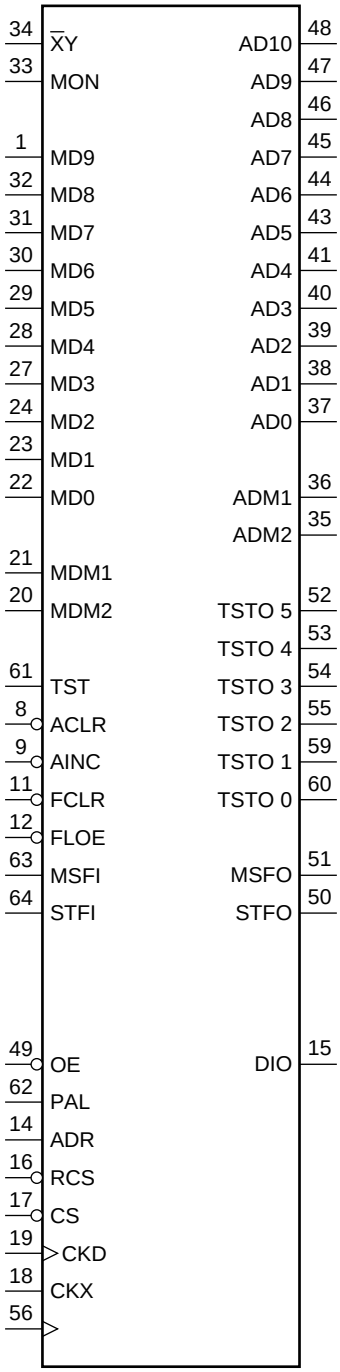
C-MOS XY ADDRESS GENERATOR

-TOP VIEW-



(V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	MD9	17	I	$\overline{CS}$	33	I	MON	49	I	$\overline{OE}$
2	—	NC	18	I	CXK	34	I	XY	50	O	STFO
3	—	NC	19	I	CXD	35	O	ADM2	51	O	MSFO
4	—	NC	20	I	MDM2	36	O	ADM1	52	O	TSO5
5	—	NC	21	I	MDM1	37	O	AD0	53	O	TSO4
6	—	NC	22	I	MD0	38	O	AD1	54	O	TSO3
7	—	NC	23	I	MD1	39	O	AD2	55	O	TSO2
8	I	$\overline{ACLR}$	24	I	MD2	40	O	AD3	56	I	CK
9	I	$\overline{AINC}$	25	—	GND	41	O	AD4	57	—	GND
10	—	GND	26	—	V_{DD}	42	—	GND	58	—	V_{DD}
11	I	$\overline{FCLR}$	27	I	MD3	43	O	AD5	59	O	TSO1
12	I	$\overline{FLOE}$	28	I	MD4	44	O	AD6	60	O	TSO0
13	—	NC	29	I	MD5	45	O	AD7	61	I	TST
14	I	ADR	30	I	MD6	46	O	AD8	62	I	PAL
15	I/O	DIO	31	I	MD7	47	O	AD9	63	I	MSFI
16	I	$\overline{RCS}$	32	I	MD8	48	O	AD10	64	I	STFI



INPUT

$\overline{ACLR}$; ADDRESS CLEAR TIMING PULSE
X MODE ····· $\overline{HD}$ INPUT (┐↓└┐)
Y MODE ····· $\overline{VD}$ INPUT (└┐↓┘)

ADR ; SERIAL ADDRESS

$\overline{AINC}$; ADDRESS INCREMENT TIMING PULSE
X MODE ····· HIGH OR LOW (FIXED)
Y MODE ····· $\overline{HD}$ INPUT (┐└┐)

CK ; SYSTEM CLOCK

CKD ; SERIAL INTERFACE CLOCK

CKX ; SWITCHING TIMING PULSE

$\overline{CS}$; CHIP SELECT (LOW : ACTIVE)

$\overline{FCLR}$; FIELD CLEAR TIMING PULSE (FOR PAL)
X MODE ····· FIELD RESET PULSE
Y MODE ····· HIGH OR LOW (FIXED)

$\overline{FLOE}$; FIELD ODD / EVEN PULSE
HIGH : EVEN FIELD

MD0 - MD9 ; 9.2 BIT DIGITAL MODULATION DATA IN (2'S COMPLEMENT)

MDM1, MDM2 ; 9.2 BIT DIGITAL MODULATION DATA IN (2'S COMPLEMENT)

MON ; MODULATION ON / OFF CONTROL
LOW : MODULATION ON

MSFI ; MULTI-SHIFT FLAG IN (LOW : ACTIVE)
Y MODE IC ····· PULL UP
X MODE IC ····· CONNECT MSFO OUT OF Y MODE IC TO MSFI OF X MODE IC

$\overline{OE}$; OUTPUT ENABLE
(LOW : ENABLE, HIGH : DISABLE)

PAL ; NTSC / PAL SELECT

$\overline{RCS}$; READ CHIP SELECT (LOW : ACTIVE)

STFI ; STREAM FLAG IN (LOW : ACTIVE)
Y MODE IC ····· PULL UP
X MODE IC ····· CONNECT STFO OUT OF Y MODE IC TO STFI OF X MODE IC

$\overline{XY}$; X (HORIZONTAL) / Y (VERTICAL) SELECT
LOW : X (HORIZONTAL) ADDRESS GENERATION MODE
HIGH : Y (VERTICAL) ADDRESS GENERATION MODE

OUTPUT

AD0 - AD10 ; 11.2 BIT ADDRESS OUT

ADM1, ADM2 ; 11.2 BIT ADDRESS OUT

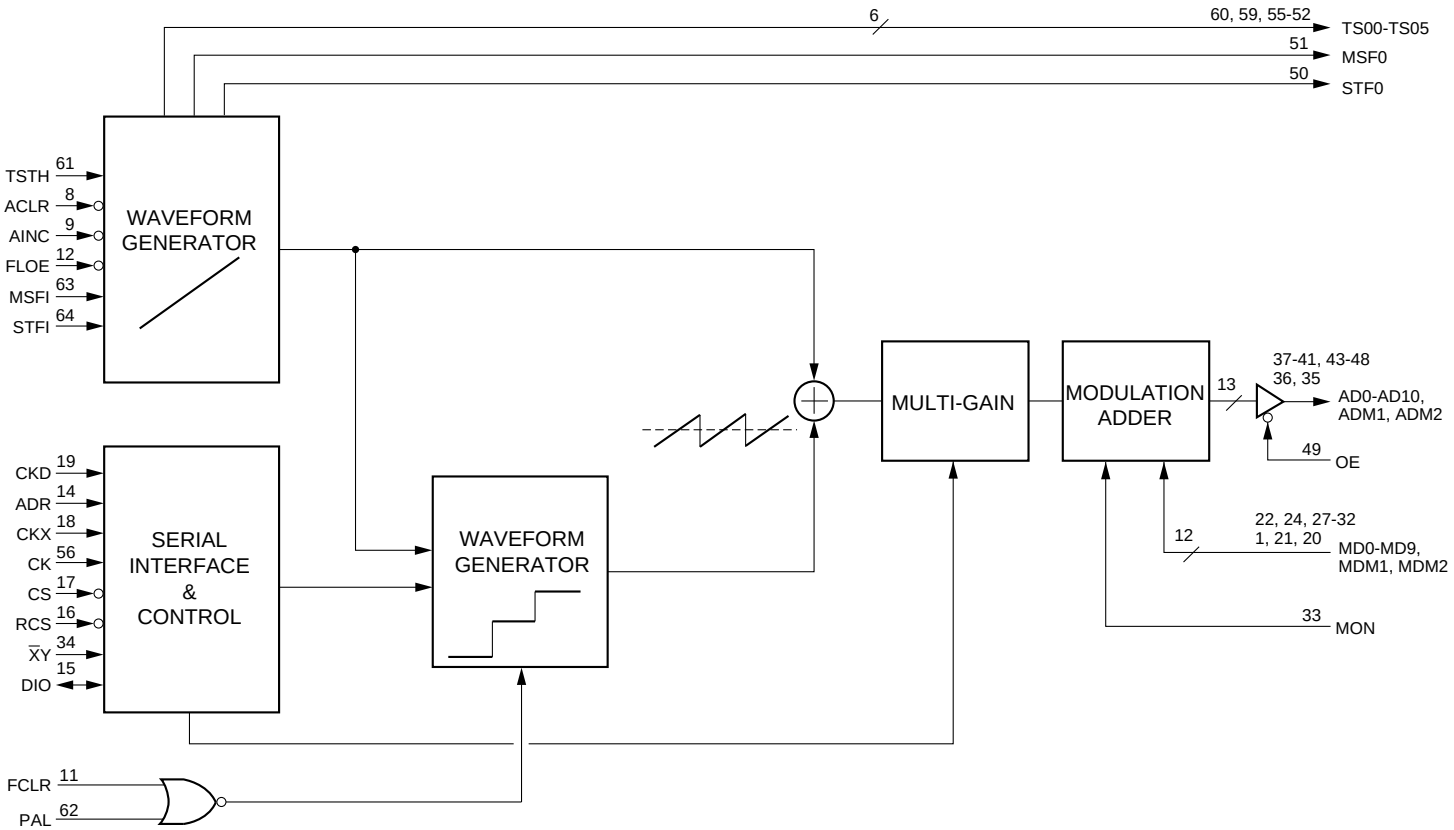
MSFO ; MULTI-SHIFT FLAG OUT (LOW : ACTIVE)

TSTO ; TEST

STFO ; STREAM FLAG OUT (LOW : ACTIVE)

INPUT / OUTPUT

DIO ; SERIAL DATA


6
60, 59, 55-52
TS00-TS05
51
MSF0
50
STF0
TSTH 61
ACLR 8
AINC 9
FLOE 12
MSFI 63
STFI 64
WAVEFORM GENERATOR
MULTI-GAIN
MODULATION ADDER
13
37-41, 43-48
36, 35
AD0-AD10,
ADM1, ADM2
49
OE
CKD 19
ADR 14
CKX 18
CK 56
CS 17
RCS 16
XY 34
DIO 15
SERIAL INTERFACE & CONTROL
WAVEFORM GENERATOR
12
22, 24, 27-32
1, 21, 20
MD0-MD9,
MDM1, MDM2
33
MON
FCLR 11
PAL 62