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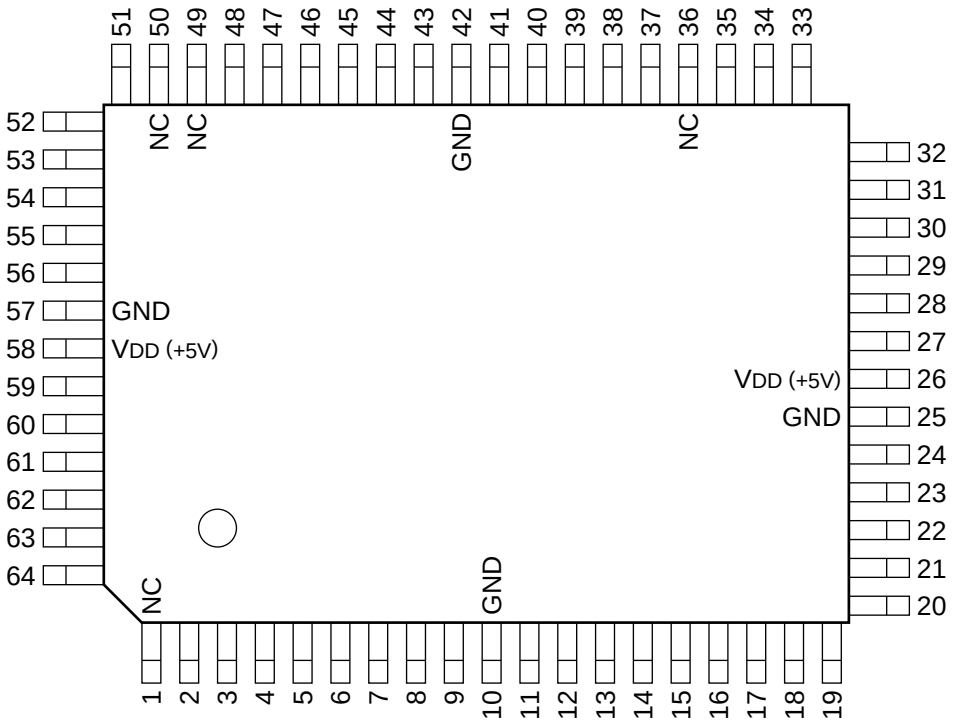
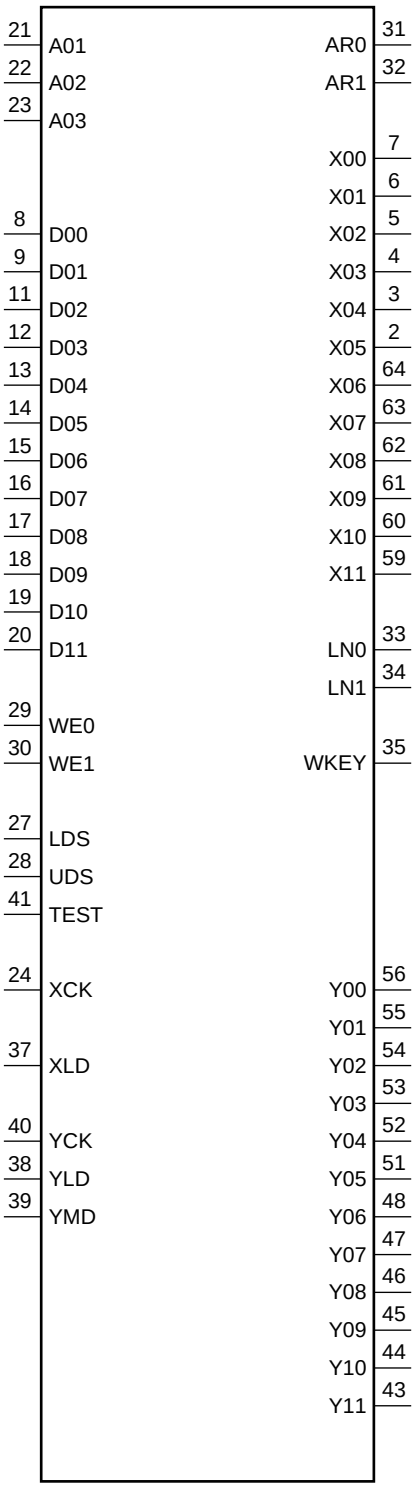
IL00

C-MOS GATE ARRAY

-TOP VIEW-



PIN NO.	I/O	SYMBOL	PIN NO.	I/O	SYMBOL	PIN NO.	I/O	SYMBOL
1	—	NC	23	I	A03	45	O	Y09
2	O	X05	24	I	XCK	46	O	Y08
3	O	X04	25	—	GND	47	O	Y07
4	O	X03	26	—	VDD (+5V)	48	O	Y06
5	O	X02	27	I	LDS	49	—	NC
6	O	X01	28	I	UDS	50	—	NC
7	O	X00	29	I	WE0	51	O	Y05
8	I	D00	30	I	WE1	52	O	Y04
9	I	D01	31	O	AR0	53	O	Y03
10	—	GND	32	O	AR1	54	O	Y02
11	I	D02	33	O	LN0	55	O	Y01
12	I	D03	34	O	LN1	56	O	Y00
13	I	D04	35	O	WKEY	57	—	GND
14	I	D05	36	—	NC	58	—	VDD (+5V)
15	I	D06	37	I	XLD	59	O	X11
16	I	D07	38	I	YLD	60	O	X10
17	I	D08	39	I	YMD	61	O	X09
18	I	D09	40	I	YCK	62	O	X08
19	I	D10	41	I	TEST	63	O	X07
20	I	D11	42	—	GND	64	O	X06
21	I	A01	43	O	Y11			
22	I	A02	44	O	Y10			



A01 - A03	;	ADDRESS 01 - 03
AR0, 1	;	VALID AREA 0, 1
D00 - D11	;	DATA INPUT 00 - 11
LDS	;	LOWER DATA STROBE
LN0, 1	;	VALID LINE 0, 1
UDS	;	UPPER DATA STROBE
TEST	;	TEST PIN
WE0, 1	;	WRITE ENABLE 0, 1
X00 - X11	;	X CONVERTER OUTPUT
XCK	;	X CLOCK
WKEY	;	WIPE KEY
XLD	;	X LOAD
Y00 - Y11	;	Y COUNTER OUTPUT 00 - 11
YCK	;	Y CLOCK
YLD	;	Y LOAD
YMD	;	Y MODE