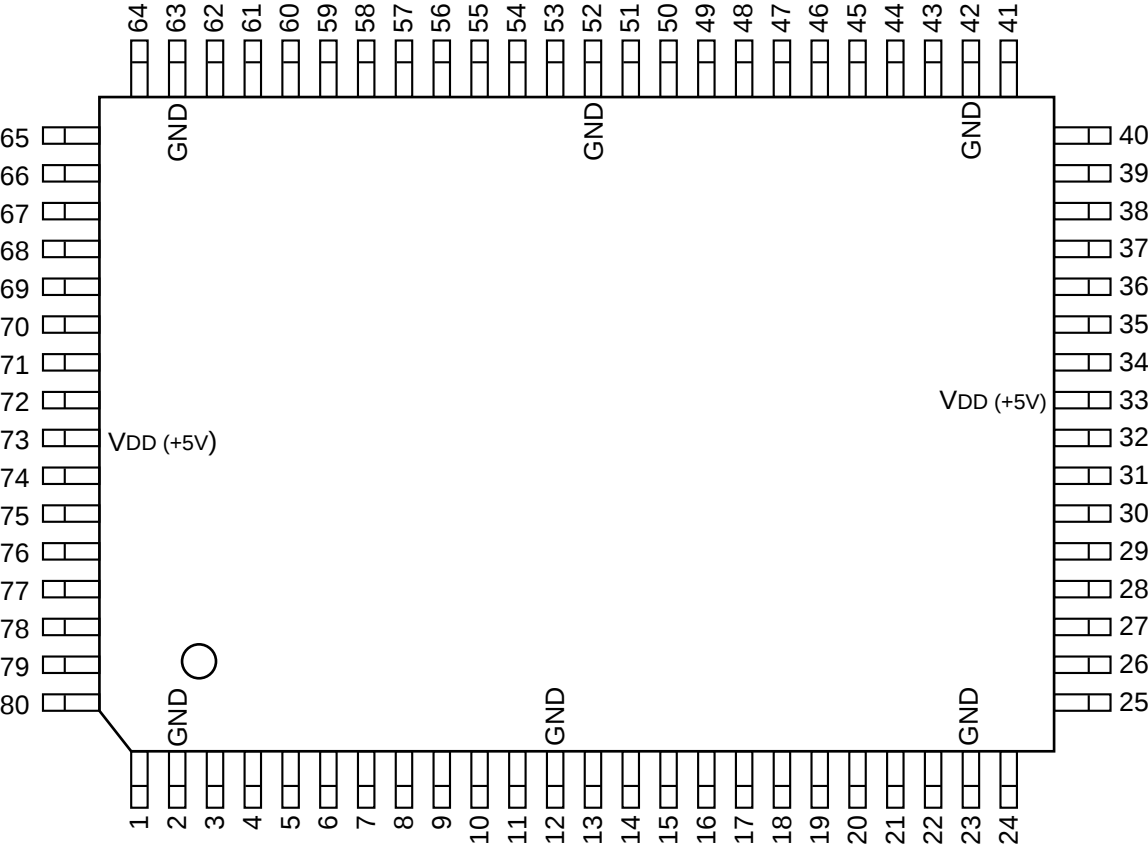


32-BIT SERIAL-PARALLEL/PARALLEL-SERIAL CONVERTER
—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	SOA	21	I/O	SDLC	41	I/O	SDRD	61	I	SIB
2	—	GND	22	I/O	SDRC	42	—	GND	62	O	SOB
3	I	SIA	23	—	GND	43	I/O	SDLD	63	—	GND
4	I/O	Q0	24	I	MODA	44	I/O	Q31	64	I	CRCD
5	I/O	Q1	25	I	MODB	45	I/O	Q30	65	I	POEB
6	I/O	Q2	26	I	THRC	46	I/O	Q29	66	I	PIEB
7	I/O	Q3	27	I	DFFC	47	I/O	Q28	67	I	PSLB
8	I/O	Q4	28	I	DIRC	48	I/O	Q27	68	I	CRCP
9	I/O	Q5	29	I	LDC	49	I/O	Q26	69	I	CRCC
10	I/O	Q6	30	I	RCKC	50	I/O	Q25	70	I	RCKB
11	I/O	Q7	31	I	SCKC	51	I/O	Q24	71	I	SCKB
12	—	GND	32	I	SCLC	52	—	GND	72	I	SCLB
13	I/O	Q8	33	—	VDD (+5V)	53	I/O	Q23	73	—	VDD (+5V)
14	I/O	Q9	34	I	SCLD	54	I/O	Q22	74	I	SCLA
15	I/O	Q10	35	I	SCKD	55	I/O	Q21	75	I	SCKA
16	I/O	Q11	36	I	RCKD	56	I/O	Q20	76	I	RCKA
17	I/O	Q12	37	I	LDD	57	I/O	Q19	77	I	PSLA
18	I/O	Q13	38	I	DIRD	58	I/O	Q18	78	I	PIEA
19	I/O	Q14	39	I	DFFD	59	I/O	Q17	79	I	POEA
20	I/O	Q15	40	I	THRD	60	I/O	Q16	80	O	CRCE

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3	SIA	Q0	4
61	SIB	Q1	5
		Q2	6
26	THRC	Q3	7
40	THRD	Q4	8
74	SCLA	Q5	9
72	SCLB	Q6	10
32	SCLC	Q7	11
34	SCLD	Q8	13
64	CRCD	Q9	14
68	CRCP	Q10	15
27	DFFC	Q11	16
39	DFFD	Q12	17
28	DIRC	Q13	18
38	DIRD	Q14	19
29	LDC	Q15	20
37	LDD	Q16	60
78	PIEA	Q17	59
66	PIEB	Q18	58
79	POEA	Q19	57
65	POEB	Q20	56
77	PSLA	Q21	55
67	PSLB	Q22	54
		Q23	53
69	CRCC	Q24	51
76	RCKA	Q25	50
70	RCKB	Q26	49
30	RCKC	Q27	48
36	RCKD	Q28	47
75	SCKA	Q29	46
71	SCKB	Q30	45
31	SCKC	Q31	44
35	SCKD		
		SOA	1
24	MODA	SOB	62
25	MODB	CRCE	80
		SDLC	21
		SDRC	22
		SDRD	41
		SDLD	43

INPUT

CRCC	; CLOCK INPUT FOR CRC CHECKER/GENERATOR
CRCD	; DATA INPUT FOR CRC CHECKER/GENERATOR
CRCP	; PRESET INPUT FOR CRC CHECKER/GENERATOR
DFFC	; DFF MODE SET FOR C BLOCK (MODE=0) PARALLEL LOAD CONTROL FOR A BLOCK SHIFT REGISTER (MODE=2)
DFFD	; DFF MODE SET FOR D BLOCK (MODE=0) PARALLEL LOAD CONTROL FOR B BLOCK SHIFT REGISTER (MODE=2) DISABLE (MODE 1,3)
DIRC	; SHIFT DIRECTION SET FOR C BLOCK SHIFT REGISTER
DIRD	; SHIFT DIRECTION SET FOR D BLOCK SHIFT REGISTER
LDC	; PARALLEL LOAD CONTROL FOR C BLOCK SHIFT REGISTER
LDD	; PARALLEL LOAD CONTROL FOR D BLOCK SHIFT REGISTER
MODA, MODB	; MODE (0,1,2,3) SET
PIEA	; PARALLEL IN ENABLE FOR AC BLOCK
PIEB	; PARALLEL IN ENABLE FOR BD BLOCK
POEA	; PARALLEL OUT ENABLE FOR AC BLOCK
POEB	; PARALLEL OUT ENABLE FOR BD BLOCK
PSLA	; PARALLEL DATA SELECT FOR AC BLOCK
PSLB	; PARALLEL DATA SELECT FOR BD BLOCK
RCKA	; CLOCK FOR A BLOCK DFF
RCKB	; CLOCK FOR B BLOCK DFF
RCKC	; CLOCK FOR C BLOCK DFF
RCKD	; CLOCK FOR D BLOCK DFF
SCKA	; CLOCK FOR A BLOCK SHIFT REGISTER
SCKB	; CLOCK FOR B BLOCK SHIFT REGISTER
SCKC	; CLOCK FOR C BLOCK SHIFT REGISTER
SCKD	; CLOCK FOR D BLOCK SHIFT REGISTER
SCLA	; ASYNCHRONOUS CLEAR FOR A BLOCK SHIFT REGISTER
SCLB	; ASYNCHRONOUS CLEAR FOR B BLOCK SHIFT REGISTER
SCLC	; ASYNCHRONOUS CLEAR FOR C BLOCK SHIFT REGISTER
SCLD	; ASYNCHRONOUS CLEAR FOR D BLOCK SHIFT REGISTER
SIA	; SERIAL DATA OUTPUT FOR A BLOCK SHIFT REGISTER
SIB	; SERIAL DATA OUTPUT FOR B BLOCK SHIFT REGISTER
THRC	; THOROUGH SET FOR C BLOCK DFF (L ; THOROUGH)
THRD	; THOROUGH SET FOR D BLOCK DFF (L ; THOROUGH)

OUTPUT

CRCE	; CHECK OUTPUT FOR CRC CHECKER/GENERATOR
SOA	; SERIAL DATA OUTPUT FOR A BLOCK SHIFT REGISTER
SOB	; SERIAL DATA OUTPUT FOR B BLOCK SHIFT REGISTER

INPUT/OUTPUT

Q0–Q7	; PARALLEL DATA FOR AC BLOCK
Q8–Q15	; PARALLEL DATA FOR AC BLOCK (MODE 0,2,3) ; PARALLEL DATA FOR BD BLOCK (MODE=1)
Q23–Q16	; PARALLEL DATA FOR BD BLOCK
Q31–Q24	; PARALLEL DATA FOR BD BLOCK
SDLC	; SERIAL DATA (L SIDE) FOR C BLOCK SHIFT REGISTER
SDRC	; SERIAL DATA (R SIDE) FOR C BLOCK SHIFT REGISTER
SDLD	; SERIAL DATA (L SIDE) FOR D BLOCK SHIFT REGISTER
SDRD	; SERIAL DATA (R SIDE) FOR D BLOCK SHIFT REGISTER

