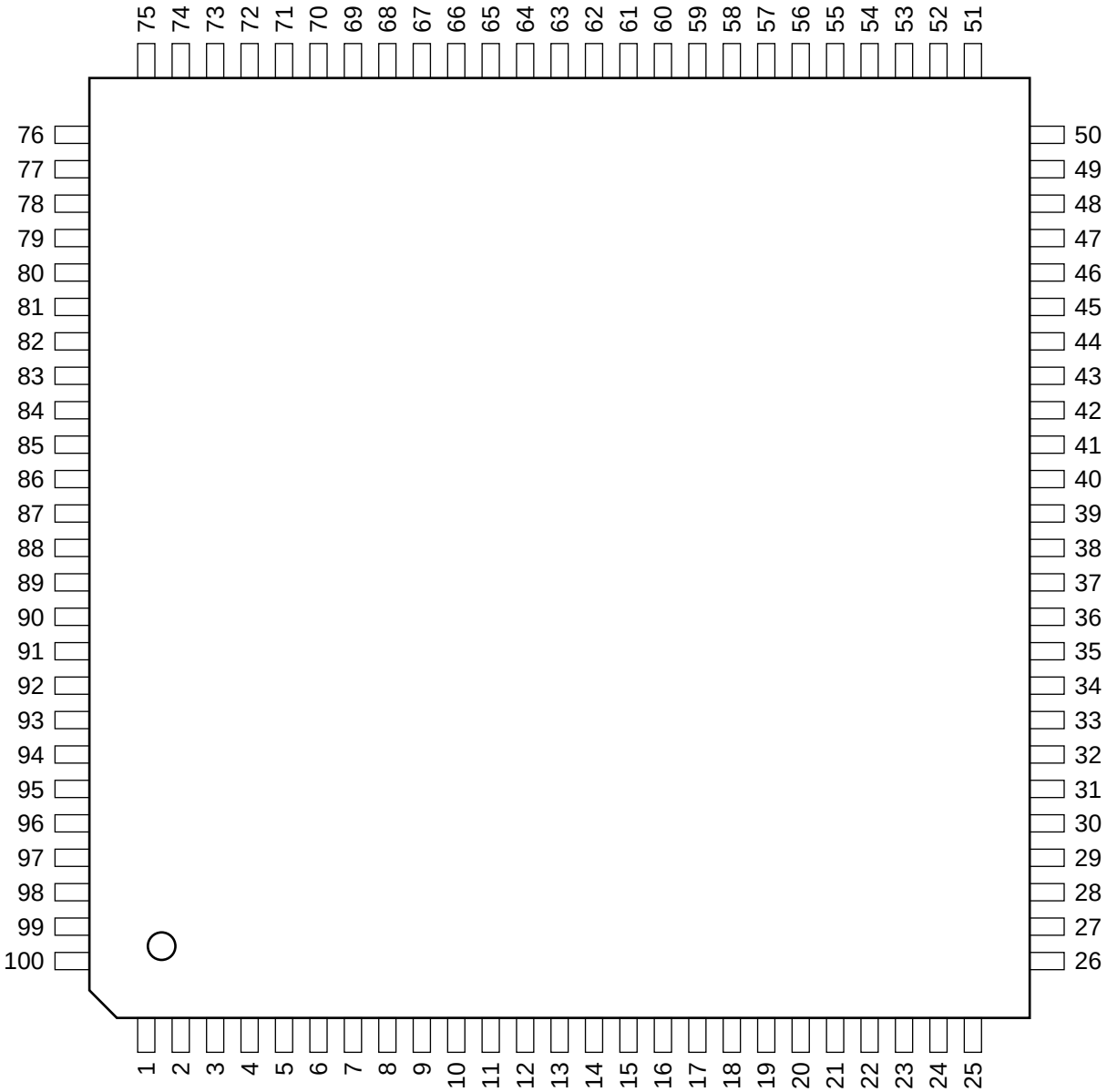
CCD SIGNAL PROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	26	—	NC	51	—	NC	76	—	NC
2	—	NC	27	—	NC	52	—	NC	77	—	NC
3	I	TEST18	28	—	GND	53	—	NC	78	—	NC
4	I	TEST19	29	O	DOC7	54	—	VCC	79	—	VCC
5	I	TEST0	30	O	DOC6	55	O	MCKO	80	I	MCKI2
6	I	INVI	31	O	DOC5	56	O	MCKO14	81	O	FRO
7	O	INVO	32	O	DOC4	57	O	MFRO	82	O	HRO
8	—	GND	33	O	DOC3	58	O	MHRO	83	O	$\overline{\text{CLPOB}}$
9	I	TEST20	34	O	DOC2	59	O	MWEO	84	I	WEI
10	I	$\overline{\text{CLR}}$	35	O	DOC1	60	O	MCKO2	85	I	MCKI
11	I	$\overline{\text{CE}}$	36	O	DOC0	61	O	TEST23	86	I	DOCNT
12	I	SCK	37	—	VCC	62	—	GND	87	—	GND
13	I	SI	38	O	DOY7	63	I	TEST7	88	I	AD9
14	O	SO	39	O	DOY6	64	I	TEST8	89	I	AD8
15	O	TEST21	40	O	DOY5	65	O	TEST9	90	I	AD7
16	—	VCC	41	O	DOY4	66	I	TEST10	91	I	AD6
17	I	TEST22	42	O	DOY3	67	I	TEST11	92	I	AD5
18	—	NC	43	O	DOY2	68	I	TEST12	93	I	AD4
19	I	TEST1	44	O	DOY1	69	I	TEST13	94	I	AD3
20	—	NC	45	O	DOY0	70	I	TEST14	95	I	AD2
21	I	TEST2	46	—	GND	71	I	TEST15	96	I	AD1
22	I	TEST3	47	I	TSTON	72	I	TEST16	97	I	AD0
23	I	TEST4	48	—	NC	73	I	TEST17	98	—	VCC
24	O	TEST5	49	—	NC	74	—	NC	99	—	NC
25	—	TEST6	50	—	NC	75	—	NC	100	—	NC

INPUTS

AD0 - AD9	: DIGITAL SIGNAL
$\overline{CE}$	: CHIP SELECT
$\overline{CLR}$	: RESET
DOCNT	: OUTPUT CONTROL
INVI	: INVERTER
MCKI2	: 2 MCKI CLOCK
MCKI	: MAIN CLOCK
SCK	: SERIAL CLOCK
SI	: SERIAL DATA
TEST0 - TEST4, TEST7, TEST8, TEST10 - TEST19, TEST20, TEST22	: TEST
TSTON	: TEST
WEI	: TG WRITE ENABLE TIMING

OUTPUTS

$\overline{CLPOB}$	: OPTICAL BLACK CLAMP PULSE
DOC0 - DOC7	: DIGITAL CHROMA
DOY0 - DOY7	: DIGITAL Y
FRO	: V SYNC FOR NEXT SIGNAL PROCESSOR
HRO	: H SYNC FOR NEXT SIGNAL PROCESSOR
INVO	: INVERTER
MCKO	: MAIN CLOCK
MCKO2	: MCKI 32
MCKO14	: 1/4 MAIN CLOCK
MFRO	: V SYNC FOR NEXT SIGNAL PROCESSOR
MHRO	: H SYNC FOR NEXT SIGNAL PROCESSOR
MWEO	: WRITE ENABLE TIMING
SO	: SERIAL DATA
TEST5, TEST9, TEST21, TEST23	: TEST

OTHERS

NC	: NO CONNECTION
TEST6	: GND