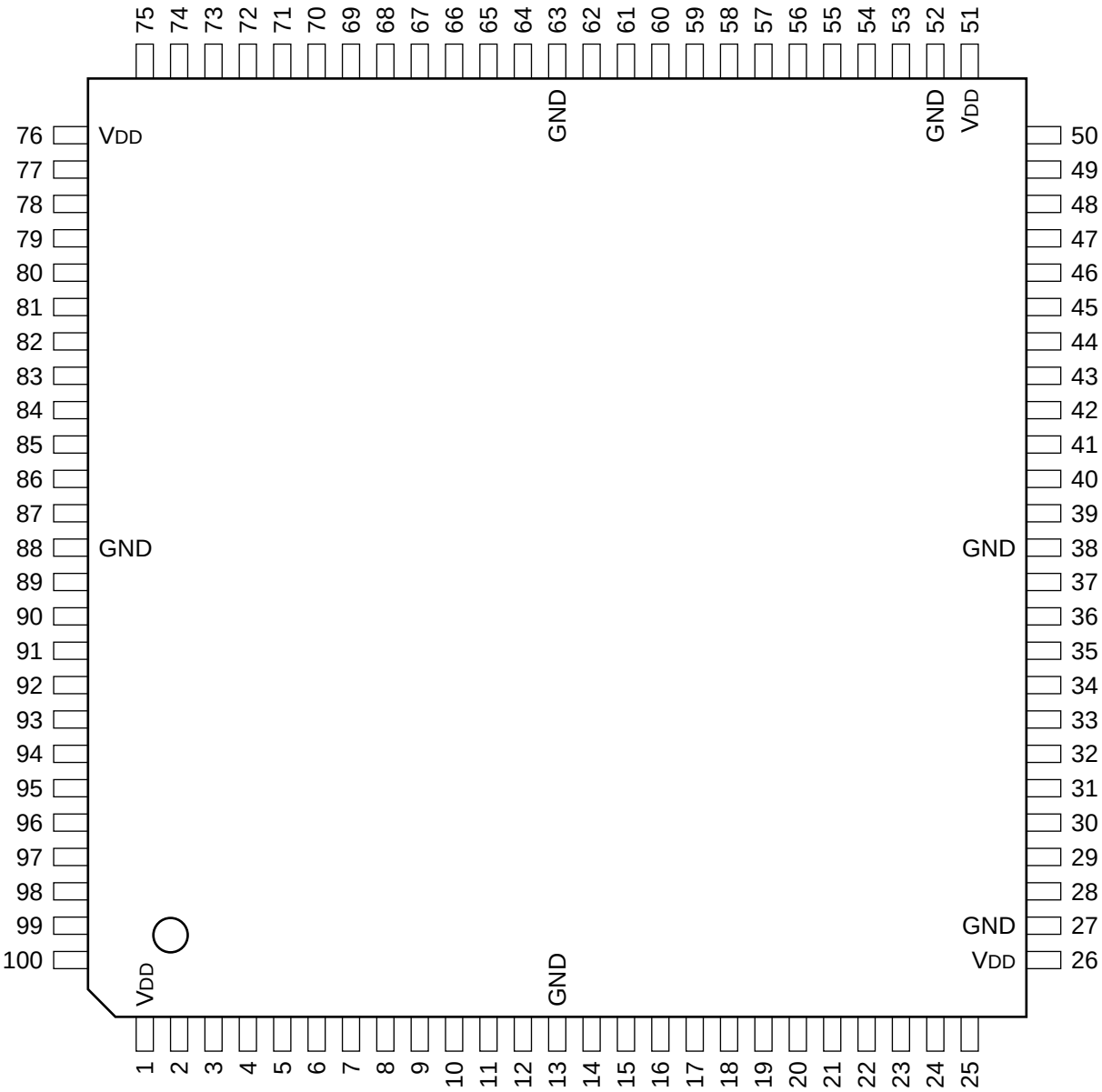
C-MOS AUDIO REC/PB SIGNAL PROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V_{DD}	26	—	V_{DD}	51	—	V_{DD}	76	—	V_{DD}
2	I/O	D7	27	—	GND	52	—	GND	77	I	$\overline{ACF}$
3	I/O	D6	28	I	FCK	53	I	TRCK	78	I	$\overline{ACT}$
4	I/O	D5	29	I/O	D3	54	I	FLTT	79	O	PBON
5	I/O	D4	30	I/O	D2	55	I	FLTA	80	O	DIIN
6	O	ERRF	31	I/O	D1	56	I/O	A14	81	I/O	A9
7	I	LRCI	32	I/O	D0	57	O	OTEN	82	I/O	A8
8	I	BCKI	33	I/O	$\overline{OE}$	58	O	SFDR	83	I/O	TSCK
9	O	LRCO	34	O	$\overline{ERS}$	59	I	STR1	84	I/O	$\overline{TSG}$
10	O	BCKO	35	O	PRST	60	I	SFP1	85	I/O	TDAT
11	O	LSBO	36	O	PCEZ	61	I	STR2	86	I	TSTM
12	O	DATO	37	O	VEN	62	I	SFP2	87	I	TSAD
13	—	GND	38	—	GND	63	—	GND	88	—	GND
14	I	DATI	39	O	$\overline{HEN}$	64	I	$\overline{RST}$	89	I	TSRM
15	I	NOIN	40	O	SLXM	65	I	$\overline{PS}$	90	I/O	A7
16	O	DSPO	41	O	SLVX	66	I/O	A13	91	I/O	A6
17	O	$\overline{ATC}$	42	O	DV32	67	I/O	A12	92	I/O	A5
18	O	ATLT	43	I/O	$\overline{WE}$	68	I/O	A11	93	I/O	A4
19	I	TCK	44	I/O	$\overline{CE}$	69	I/O	A10	94	I/O	A3
20	I	TENA3	45	I	MDPL	70	I	$\overline{SCK}$	95	I/O	A2
21	I	TDI	46	O	$\overline{REF}$	71	I	SPSO	96	I/O	A1
22	I	TENA1	47	O	$\overline{VAR}$	72	O	SPSI	97	I/O	A0
23	O	TDO	48	O	$\overline{INT}$	73	I	$\overline{MUT}$	98	O	FSE2
24	I	TRST	49	I	JRDY	74	I	$\overline{DSP}$	99	O	FSE1
25	I	VST	50	I	JDAT	75	I	$\overline{ATT}$	100	O	EMPA

INPUT

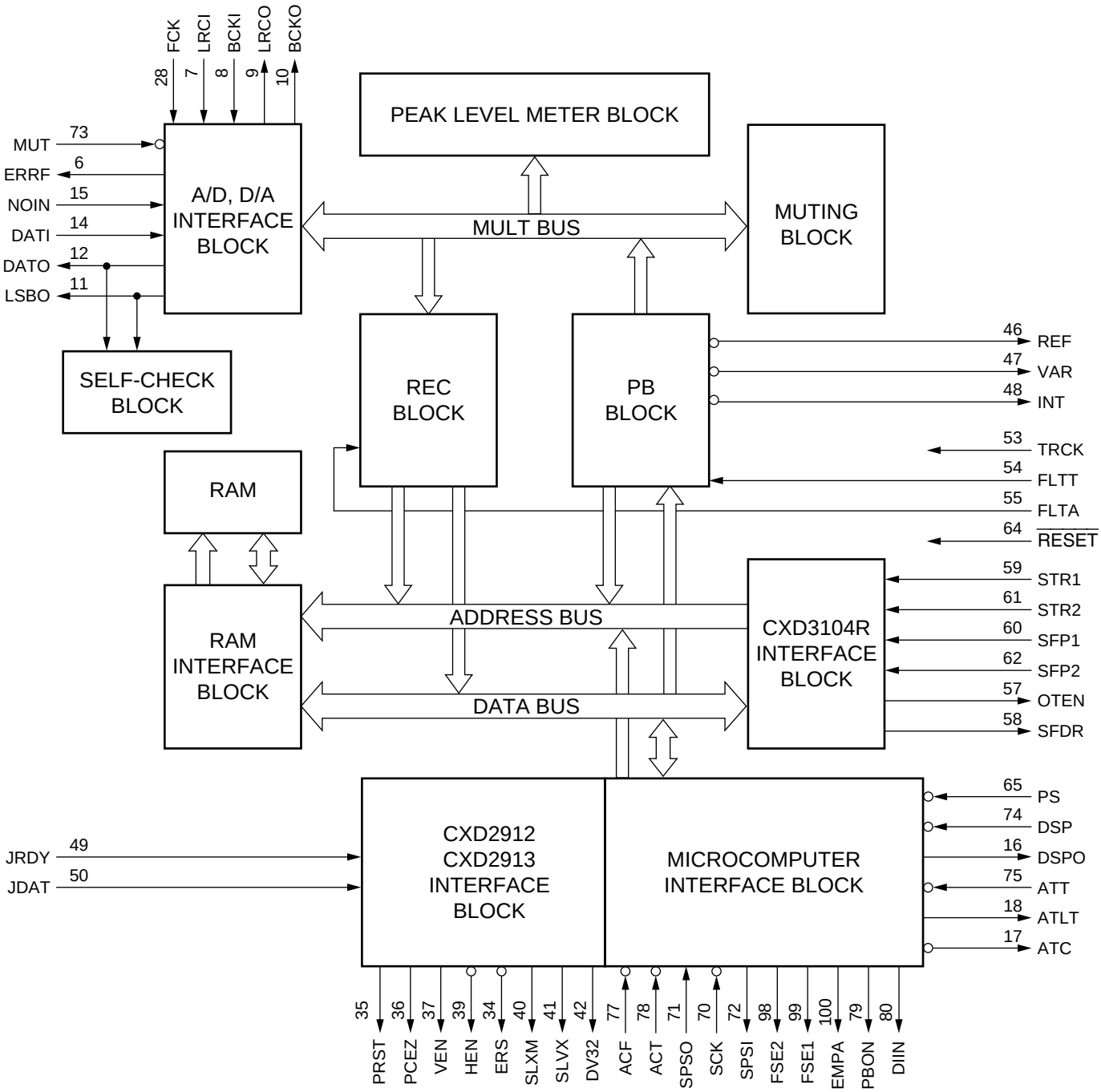
$\overline{ACF}$	:	MICROCOMPUTER FRAME COMMUNICATION CHIP SELECT
$\overline{ACT}$	:	MICROCOMPUTER TRACK-PAIR COMMUNICATION CHIP SELECT
$\overline{ATT}$	:	AUTO ATT INTERFACE CHIP SELECT
BCKI	:	64 FS SIGNAL
DATI	:	AUDIO DATA
$\overline{DSP}$	:	ADSP INTERFACE CHIP SELECT
FCK	:	256 FS CLOCK
FLTA	:	RECORDING FRAME SIGNAL
FLTT	:	TRANSFER/PLAYBACK FRAME SIGNAL
JDAT	:	INTERFACE
JRDY	:	INTERFACE
LRCI	:	FS SIGNAL
MDPL	:	(FOR TEST)
$\overline{MUT}$	:	DIRECT MUTING
NOIN	:	D/A THROUGH MODE AUDIO DATA
$\overline{PS}$	:	POWER SAVE MODE
$\overline{RST}$	:	RESET
$\overline{SCK}$	:	MICROCOMPUTER TRANSFER CLOCK
SFP1, SFP2	:	PLAYBACK DATA
SPSO	:	MICROCOMPUTER COMMUNICATION DATA
STR1, STR2	:	REC/PB DATA COMMUNICATION START PULSE
TCK	:	(FOR TEST)
TDI	:	(FOR TEST)
TENA1, TENA3	:	(FOR TEST)
TRCK	:	MAIN CLOCK
TRST	:	(FOR TEST)
TSAD	:	(FOR TEST)
TSRM	:	(FOR TEST)
TSTM	:	(FOR TEST)
VST	:	(FOR TEST)

OUTPUT

$\overline{ATC}$	:	AUTO ATT INTERFACE CLOCK
ATLT	:	AUTO ATT INTERFACE LATCH PULSE
BCKO	:	64 FS SIGNAL
DATO	:	AUDIO DATA (MSB FIRST FORMAT)
DIIN	:	MICROCOMPUTER INTERFACE SERIAL/PARALLE CONVERSION
DSPO	:	ADSP INTERFACE CLOCK
DV32	:	INTERFACE
EMPA	:	MICROCOMPUTER INTERFACE SERIAL/PARALLEL CONVERSION
ERRF	:	PB AUDIO DATA ERROR RECOGNITION SIGNAL
$\overline{ERS}$	:	RESET
FSE1, FSE2	:	MICROCOMPUTER INTERFACE SERIAL/PARALLEL CONVERSION
$\overline{HEN}$	:	INTERFACE
$\overline{INT}$	:	PLAYBACK PHASE CHECKING
LRCO	:	FS SIGNAL
LSBO	:	AUDIO DATA (LSB FIRST FORMAT)
OTEN	:	RECORDING DATA COMMUNICATION ENABLE
PBON	:	MICROCOMPUTER INTERFACE SERIAL/PARALLEL CONVERSION
PCEZ	:	INTERFACE
PRST	:	INTERFACE
$\overline{REF}$	:	PHASE COMPARATOR REFERENCE CLOCK
SFDR	:	RECORDING DATA
SLVX	:	INTERFACE
SLXM	:	INTERFACE
SPSI	:	MICROCOMPUTER COMMUNICATION DATA
TDO	:	(FOR TEST)
$\overline{VAR}$	:	PHASE COMPARATOR COMPARISON CLOCK
VEN	:	INTERFACE

INPUT/OUTPUT

A0 - A14	:	(FOR TEST)
$\overline{CE}$	:	(FOR TEST)
D0 - D7	:	(FOR TEST)
$\overline{OE}$	:	(FOR TEST)
TDAT	:	(FOR TEST)
TSCK	:	(FOR TEST)
$\overline{TSG}$	:	(FOR TEST)
$\overline{WE}$	:	(FOR TEST)


FCK
LRCI
BCKI
LRCO
BCKO
28
7
8
9
10
PEAK LEVEL METER BLOCK
MUT
73
ERRF
6
NOIN
15
DATI
14
DATO
12
LSBO
11
A/D, D/A
INTERFACE
BLOCK
MULT BUS
MUTING
BLOCK
SELF-CHECK
BLOCK
REC
BLOCK
PB
BLOCK
46
REF
47
VAR
48
INT
53
TRCK
54
FLTT
55
FLTA
64
RESET
RAM
RAM
INTERFACE
BLOCK
ADDRESS BUS
DATA BUS
CXD3104R
INTERFACE
BLOCK
59
STR1
61
STR2
60
SFP1
62
SFP2
57
OTEN
58
SFDR
JRDY
49
JDAT
50
CXD2912
CXD2913
INTERFACE
BLOCK
MICROCOMPUTER
INTERFACE BLOCK
65
PS
74
DSP
16
DSPO
75
ATT
18
ATLT
17
ATC
35
PRST
36
PCEZ
37
VEN
39
HEN
34
ERS
40
SLXM
41
SLVX
42
DV32
77
ACF
78
ACT
71
SPSO
70
SCK
72
SPSI
98
FSE2
99
FSE1
100
EMPA
79
PBON
80
DIIN