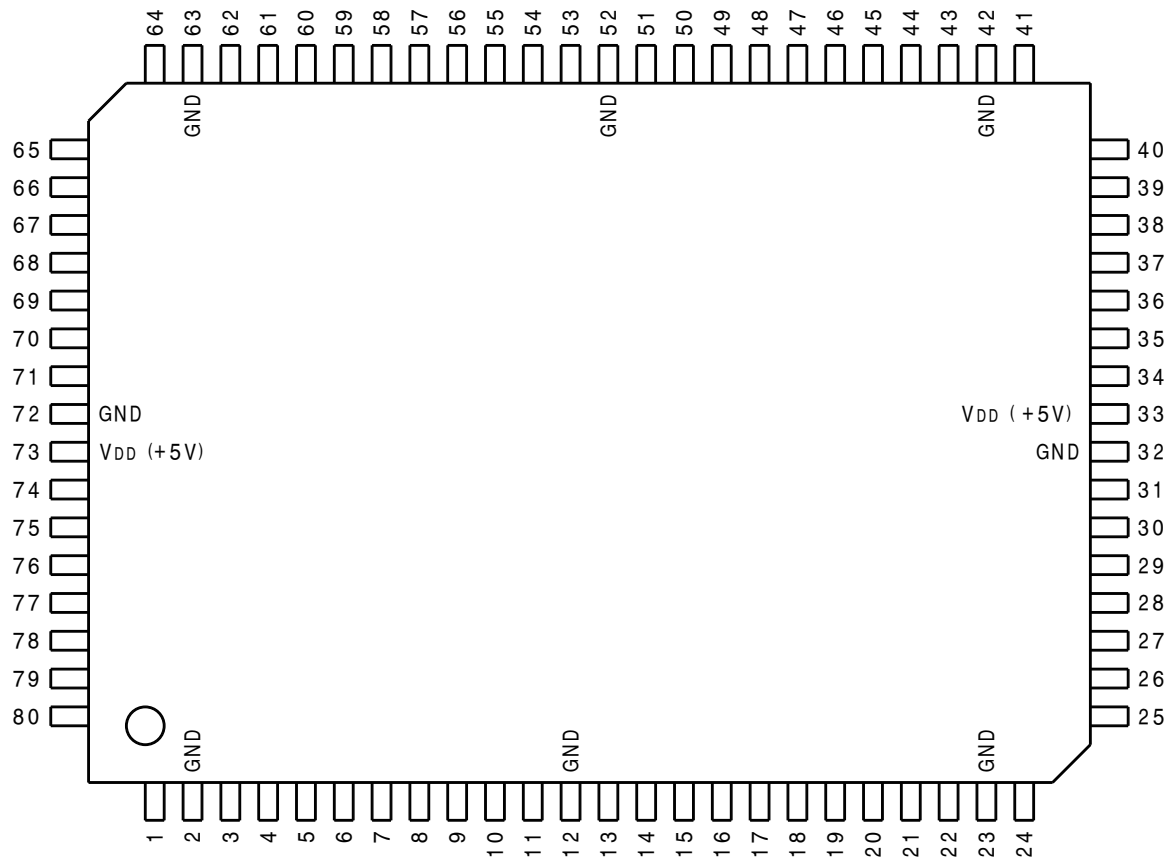

C-MOS DIGITAL AUDIO SIGNAL PROCESSOR

-TOP VIEW-



(VDD =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	TST I	21	O	HD7	41	-	NC	61	-	NC
2	-	GND	22	O	HD8	42	-	GND	62	-	NC
3	I	TEST	23	-	GND	43	-	NC	63	-	GND
4	I	PSSL	24	O	HD9	44	-	NC	64	-	NC
5	I	HA0	25	O	HD10	45	O	A0	65	-	NC
6	I	HA1	26	O	HD11	46	O	A1	66	-	NC
7	I	HA2	27	I	SIA	47	O	A2	67	-	NC
8	I	HA3	28	O	SOA	48	O	A3	68	O	XRAS
9	I	XRD	29	I	BCK	49	O	A4	69	O	XWSO
10	I	MCK1	30	I	LRCK	50	O	A5	70	I/O	DIO
11	I	MCK2	31	O	OVR	51	O	A6	71	O	XCAS
12	-	GND	32	-	GND	52	-	GND	72	-	GND
13	I	H16B	33	-	VDD	53	O	A7	73	-	VDD
14	O	HD0	34	I	XCLR	54	O	A8	74	I	SDT I
15	O	HD1	35	I	SIB	55	O	A9	75	I	SCK
16	O	HD2	36	O	SOB	56	O	A10	76	I	XSLD
17	O	HD3	37	O	HD12	57	I	TSTJ	77	O	XRDY
18	O	HD4	38	O	HD13	58	I	SBCK	78	O	SDTO
19	O	HD5	39	O	HD14	59	I	SLC	79	I	XCS
20	O	HD6	40	O	HD15	60	-	NC	80	-	NC

79	XCS	SDTO	78	BCK	: SERIAL DATA TRANSMISSION CLOCK
75	SCK	XRDY	77	H16B	: TEST PIN. NORMALLY FIXED AT "L"
76	XSLD			HA0-HA3	: TEST PIN. NORMALLY FIXED AT "L"
74	SDTI	SOA	28	LRCK	: SERIAL I/O SAMPLING RATE CLOCK INPUT
		SOB	36	MCK1	: MASTER CLOCK INPUT 1
27	SIA	OVR	31	MCK2	: MASTER CLOCK INPUT 2
35	SIB			PSSL	: TEST PIN. NORMALLY FIXED AT "L"
		HD0	14	SBCK	: TEST PIN. NORMALLY FIXED AT "L"
1	TSTI	HD1	15	SCK	: MICROPROCESSOR INTERFACE SERIAL TRANSMISSION CLOCK
3	TEST	HD2	16	SDTI	: MICROPROCESSOR INTERFACE SERIAL DATA INPUT
4	PSSL	HD3	17	SIA	: 2-CHANNEL SERIAL DATA INPUT A
5	HA0	HD4	18	SIB	: 2-CHANNEL SERIAL DATA INPUT B
6	HA1	HD5	19	SLC	: TEST PIN. NORMALLY FIXED AT "L"
7	HA2	HD6	20	TEST	: TEST PIN. NORMALLY FIXED AT "L"
8	HA3	HD7	21	TSTI	: TEST PIN. NORMALLY FIXED AT "L"
9	XRD	HD8	22	TSTJ	: TEST PIN. NORMALLY FIXED AT "L"
		HD9	24	XCLR	: TEST PIN. NORMALLY FIXED AT "H"
13	H16B	HD10	25	XCS	: MICROPROCESSOR INTERFACE CHIP SELECT
		HD11	26	XRD	: TEST PIN. NORMALLY FIXED AT "L"
29	BCK	HD12	37	XSLD	: MICROPROCESSOR INTERFACE SERIAL DATA INPUT LATCH
30	LRCK	HD13	38		
		HD14	39		
34	XCLR	HD15	40		
57	TSTJ				
58	SBCK	XWSO	69	SDTO	: MICROPROCESSOR INTERFACE SERIAL DATA OUTPUT
59	SLC	DIO	70	SOA	: 2-CHANNEL SERIAL DATA OUTPUT A
		XRAS	68	SOB	: 2-CHANNEL SERIAL DATA OUTPUT B
10	MCK1	XCAS	71	XCAS	: EXTERNAL DRAM COLUMN ADDRESS STROBE OUTPUT
11	MCK2			XRAS	: EXTERNAL DRAM LOW ADDRESS STROBE OUTPUT
		A0	45	XRDY	: MICROPROCESSOR INTERFACE TRANSMISSION READY
		A1	46	XWSO	: EXTERNAL DRAM READ/WRITE OUTPUT
		A2	47		
		A3	48		
		A4	49		
		A5	50		
		A6	51		
		A7	53		
		A8	54		
		A9	55		
		A10	56		

INPUT	
BCK	: SERIAL DATA TRANSMISSION CLOCK
H16B	: TEST PIN. NORMALLY FIXED AT "L"
HA0-HA3	: TEST PIN. NORMALLY FIXED AT "L"
LRCK	: SERIAL I/O SAMPLING RATE CLOCK INPUT
MCK1	: MASTER CLOCK INPUT 1
MCK2	: MASTER CLOCK INPUT 2
PSSL	: TEST PIN. NORMALLY FIXED AT "L"
SBCK	: TEST PIN. NORMALLY FIXED AT "L"
SCK	: MICROPROCESSOR INTERFACE SERIAL TRANSMISSION CLOCK
SDTI	: MICROPROCESSOR INTERFACE SERIAL DATA INPUT
SIA	: 2-CHANNEL SERIAL DATA INPUT A
SIB	: 2-CHANNEL SERIAL DATA INPUT B
SLC	: TEST PIN. NORMALLY FIXED AT "L"
TEST	: TEST PIN. NORMALLY FIXED AT "L"
TSTI	: TEST PIN. NORMALLY FIXED AT "L"
TSTJ	: TEST PIN. NORMALLY FIXED AT "L"
XCLR	: TEST PIN. NORMALLY FIXED AT "H"
XCS	: MICROPROCESSOR INTERFACE CHIP SELECT
XRD	: TEST PIN. NORMALLY FIXED AT "L"
XSLD	: MICROPROCESSOR INTERFACE SERIAL DATA INPUT LATCH
OUTPUT	
A0-A10	: EXTERNAL DRAM ADDRESS OUTPUT A0-A10
HD0-HD15	: TEST PIN. NORMALLY FIXED AT "H"
OVR	: CALCULATOR OVERFLOW DETECTION OUTPUT
SDTO	: MICROPROCESSOR INTERFACE SERIAL DATA OUTPUT
SOA	: 2-CHANNEL SERIAL DATA OUTPUT A
SOB	: 2-CHANNEL SERIAL DATA OUTPUT B
XCAS	: EXTERNAL DRAM COLUMN ADDRESS STROBE OUTPUT
XRAS	: EXTERNAL DRAM LOW ADDRESS STROBE OUTPUT
XRDY	: MICROPROCESSOR INTERFACE TRANSMISSION READY
XWSO	: EXTERNAL DRAM READ/WRITE OUTPUT
INPUT/OUTPUT	
DIO	: EXTERNAL DRAM DATA INPUT/OUTPUT