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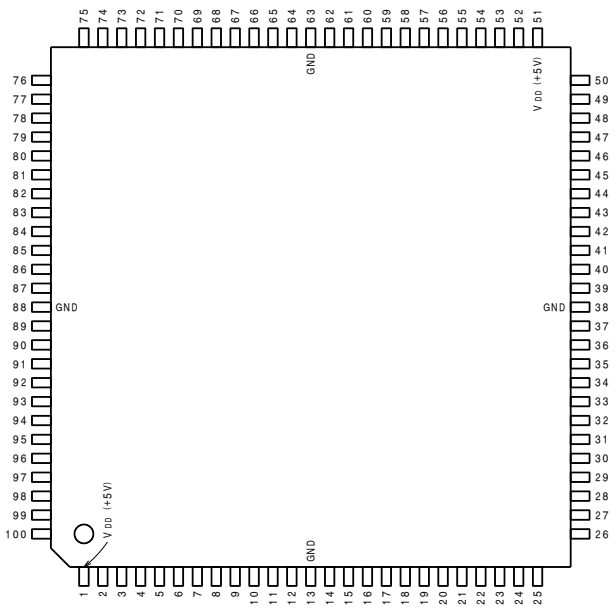
C-MOS SIGNAL PROCESSOR FOR R-DAT

-TOP VIEW-



(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	–	V_{DD}	26	O	CCLK	51	–	V_{DD}	76	I	DADO
2	O	A10	27	I	MUTE	52	O	TX	77	O	ADDI
3	O	A11	28	O	MUTM	53	I	TST6	78	I	ADDN
4	O	A12	29	O	UNLK	54	I/O	EXSY	79	I	ERRI
5	O	A13	30	I	RFCT	55	I/O	EXSN	80	O	ERRF
6	O	A14	31	O	SYMN	56	I/O	F128	81	O	MNTG
7	O	XWE	32	I	TST5	57	O	F256	82	I/O	D7
8	O	XOE	33	O	PLCK	58	O	F512	83	I/O	D6
9	O	XEAN	34	I	TST2	59	I	ADLF	84	I/O	D5
10	I	TST1	35	I	RFDT	60	I	DALF	85	I/O	D4
11	O	XT1O	36	I	XCS	61	O	XT2O	86	I/O	D3
12	I	XT1I	37	I	SWP	62	I	XT2I	87	I/O	D2
13	–	GND	38	–	GND	63	–	GND	88	–	GND
14	I	XRST	39	O	PIPC	64	O	XT3O	89	I/O	D1
15	O	CLKO	40	O	REPB	65	I	XT3I	90	I/O	D0
16	O	MINT	41	O	REDT	66	I	FSEN	91	O	A00
17	I	ATSY	42	I	TST4	67	O	LR03	92	O	A01
18	O	MCLK	43	O	PDO	68	O	LR02	93	O	A02
19	O	DREF	44	I	SELC	69	O	LR01	94	O	A03
20	O	SBPM	45	I	MUTA	70	I/O	LRCK	95	O	A04
21	I	EXCK	46	I	PLCO	71	O	WCK	96	O	A05
22	I	SDSI	47	O	PLVR	72	O	XBCK	97	O	A06
23	O	SDSO	48	O	PLRF	73	I/O	BCK	98	O	A07
24	O	SBSY	49	I	MSSL	74	I	ADDT	99	O	A08
25	O	RFPL	50	I	RX	75	O	DADT	100	O	A09

INPUT

ADDN	;AUDIO SIGNAL FOR AES/EBU DIGITAL IN. NORMALLY CONNECTED TO ADDI
ADDT	;SERIAL DATA FROM ADC. SYNCHRONIZES WITH BCK
ADLF	;LSB-MSB FIRST SELECTION FOR ADDT/ADDN/ADDI SIGNALS. LSB FIRST IS SELECTED WHEN "H"
ATSY	;ATF SYNC SIGNAL. SYNCHRONIZES WHEN "H"
DALF	;LSB/MSB FIRST SELECTION FOR DADT/DADO SIGNALS. LSB FIRST WHEN "H"
DADO	;AUDIO SIGNAL FOR AES/EBU DIGITAL OUT. NORMALLY CONNECTED TO DADT
ERRI	;VALIDITY FLAG FOR AES/EBU DIGITAL OUT. NORMALLY CONNECTED TO ERRF
EXCK	;CLOCK FOR DATA TRANSMISSION WITH µCOM
FSEN	;F128, BCK, LRCK INPUT/OUTPUT SELECTION. OUTPUT WHEN "H"
MSSL	;MASTER/SLAVE SELECTION. MASTER WHEN "H"
MUTA	;MUTES REC MONITOR SOUNDS AS WELL. 49.152MHz WHEN "H"
MUTE	;DOES NOT MUTE REC MONITOR SOUNDS. MUTES WHEN "H"
PLCO	;RX-ANALOG PLL EXTERNAL VCO CLOCK INPUT
RFCT	;RF SIGNAL CUT CONTROL. CUTS WHEN "H"
RFDT	;PLAYBACK RF SIGNAL
RX	;AES/EBU DIGITAL IN SIGNAL
SDSI	;SERIAL DATA INPUT FROM µCOM
SDSO	;SERIAL DATA OUTPUT TO µCOM
SELC	;CRYSTAL 3 LIQUID C
SWP	;PLAYBACK RF SIGNAL DISCRIMINATION. A CH TRACK WHEN "L" AND B CH TRACK WHEN "H"
TST1	;TEST PIN.FIXED AT "L"
TST2	;TEST PIN.FIXED AT "L"
TST4	;TEST PIN.FIXED AT "L"
TST5	;TEST PIN.FIXED AT "H"
TST6	;TEST PIN.FIXED AT "H"
XCS	;CHIP SELECT FOR DATA TRANSMISSION WITH µCOM. TRANSMISSION PERMITTED WHEN "L"
XRST	;RESET INPUT. RESETS WHEN "L"
XT1I	;CRYSTAL OSCILLATION CIRCUIT 1 INPUT
XT2I	;CRYSTAL OSCILLATION CIRCUIT 2 INPUT
XT3I	;CRYSTAL OSCILLATION CIRCUIT 3 INPUT

OUTPUT

A00-A14	;EXTERNAL RAM ADDRESS OUTPUT
ADDI	;AUDIO SIGANL FOR AES/EBU DIGITAL IN
CCLK	;9.8304MHz/12.288MHz
CLKO	;SYSTEM CLOCK OUTPUT (4.9152MHz/8.192MHz)
DADT	;SERIAL DATA TO DAC
DREF	;SIGNAL WITH SBSY PERIOD AND 50% DUTY
ERRF	;DADT DATA COMPENSATION DISCRIMINATION SIGNAL. COMPENSATION DATA WHEN "H"
F256	;256xfs.512xfs WHEN DOUBLE SPEED
F512	;512xfs.DOES NOT CHANGE EVEN WHEN DOUBLE SPEED
LRO1	;15BCK DELAY SIGNAL OF LRCK
LRO2	;16BCK DELAY SIGNAL OF LRCK/LRCK CLOCK OF RX-PLL
LRO3	;LRO2 REVERSAL SIGNAL
MCLK	;CHANNEL CLOCK OUTPUT
MINT	;SIGNAL DETECTING INTERVAL BETWEEN PROGRAMS (CD) (AT DIN)/RX-PLL BCK CLOCK
MNTG	;D0 to D7 CORRECTION MONITOR DATA DISCRIMINATION SIGNAL. VALID WHEN "H"
MUTM	;MUTE MONITOR. MUTES WHEN "H"
PDO	;PHASE COMPARATOR OUTPUT FOR RX-ANALOG PLL
PIPC	;ATF PILOT SIGNAL DISCRIMINATION OF RECORDING SIGNALS. PILOT SIGNAL WHEN "H"
PLCK	;RF-PLL CLOCK/RX-PLL F128 CLOCK
PLRF	;RX-ANALOG PLL PHASE COMPARISON SIGNAL (2fs RX SYNC DETECTION SIGNAL)
PLVR	;RX-ANALOG PLL PHASE COMPARISON SIGNAL (2fs FROM THE PLL CLOCK)
REDT	;RECORDING SIGNAL
REPB	;REC-PB DISCRIMINATION SIGNAL. REC WHEN "H"
RFPL	;1/5880 FREQUENCY DIVISION OF PLL CLOCK
SBPM	;SIGNAL PERMITTING PACK TRANSMISSION WITH µCOM/RX-PLL F256 CLOCK
SBSY	;FRAME SYNC SIGNAL OUTPUT FOR DATA TRANSMISSION WITH µCOM
SYMN	;C1 CHECK RESULTS CORRESPONDING TO RF. "OK" WHEN "H"
TX	;AES/EBU DIGITAL OUT SIGNAL
UNLK	;RX-PLL LOCK MONITOR SIGNAL. LOCKS WHEN "L"
WCK	;2xfs, 4xfs WHEN DOUBLE SPEED
XBCK	;BCK REVERSAL SIGNAL
XEAN	;EXTERNAL ADDRESSING ENABLE SIGNAL OUTPUT
XOE	;EXTERNAL RAM OUTPUT ENABLE SIGNAL OUTPUT
XT1O	;CRYSTAL OSCILLATION CIRCUIT 1 OUTPUT (9.408MHz/18.816MHz/37.632MHz)
XT2O	;CRYSTAL OSCILLATION CIRCUIT 2 OUTPUT (22.5792MHz)
XT3O	;CRYSTAL OSCILLATION CIRCUIT 3 OUTPUT (24.576MHz/49.152MHz)
XWE	;EXTERNAL RAM WRITE ENABLE SIGNAL OUTPUT

INPUT/OUTPUT

BCK	;64xfs 128xfs WHEN DOUBLE SPEED
D0-D7	;EXTERNAL RAM DATA
EXSN	;EXTERNAL SYNC SIGNAL. NORMALLY CONNECTED TO EXSY
EXSY	;EXTERNAL SYNC SIGNAL. NORMALLY CONNECTED TO EXSN (x1SP:100/3Hz)
F128	;128xfs.256xfs WHEN DOUBLE SPEED
LRCK	;fs, 2xfs WHEN DOUBLE SPEED