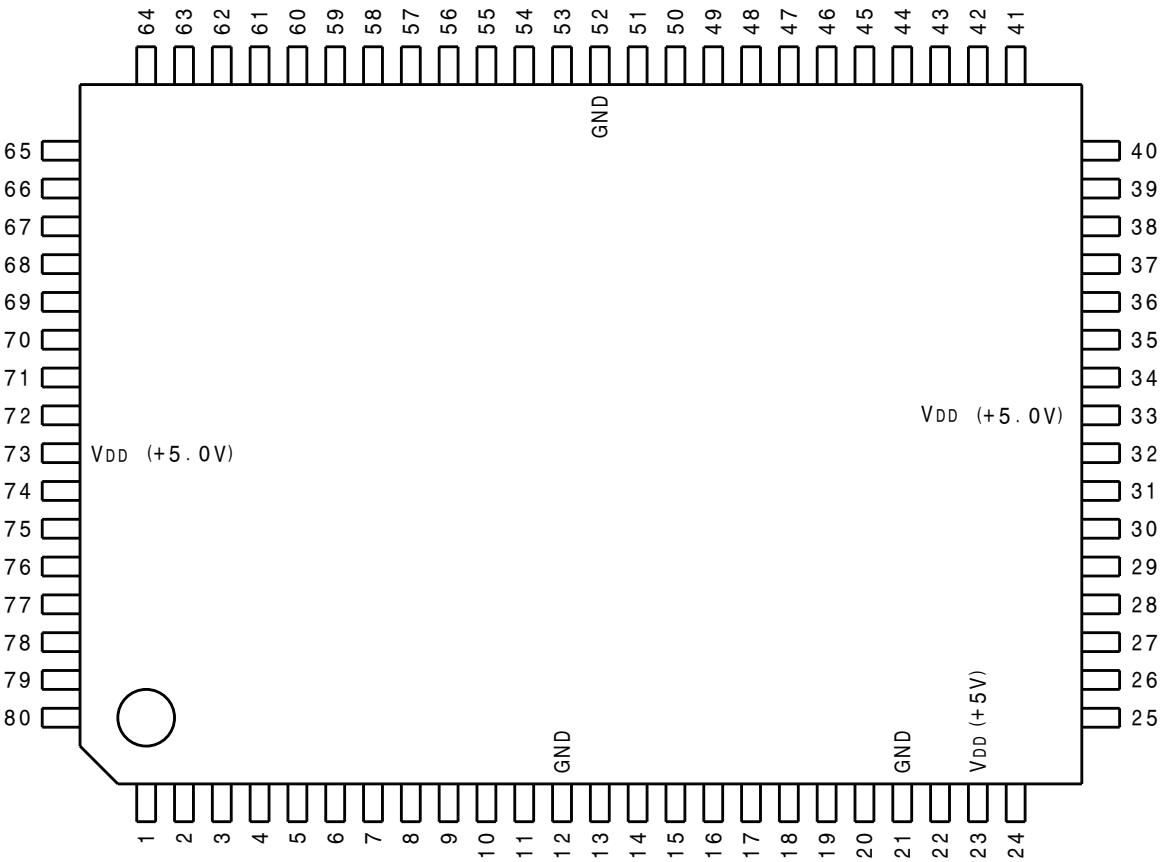
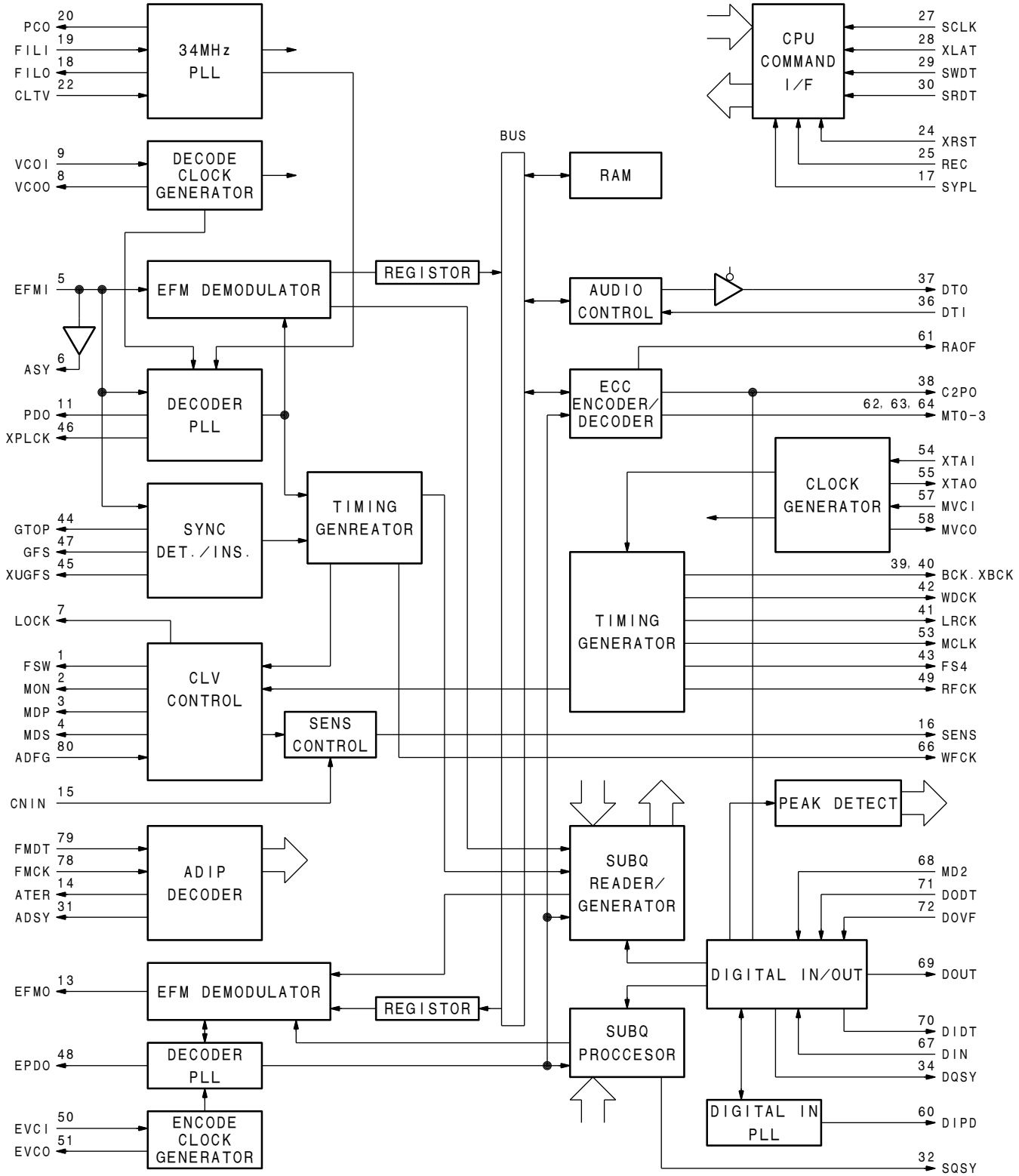
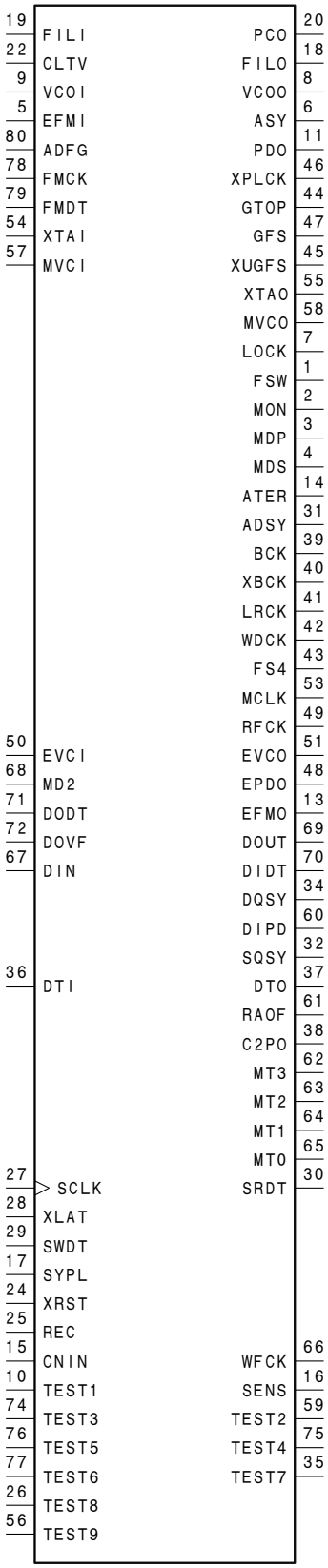
EFM ·ACIRC ENCODER/DECODER

-TOP VIEW-



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	FSW	21	–	GND	41	O	LRCK	61	O	RAOF
2	O	MON	22	I	CLTV	42	O	WDCK	62	O	MT3
3	O	MDP	23	–	VDD	43	O	FS4	63	O	MT2
4	O	MDS	24	I	XRST	44	O	GTOP	64	O	MT1
5	I	EFMI	25	I	REC	45	O	XUGFS	65	O	MT0
6	O	ASY	26	I	TEST8	46	O	XPLCK	66	O	WFCK
7	O	LOCK	27	I	SCLK	47	O	GFS	67	I	DIN
8	O	VCOO	28	I	XLAT	48	O	EPDO	68	I	MD2
9	I	VCOI	29	I	SWDT	49	O	RFCK	69	O	DOUT
10	I	TEST1	30	O	SRDT	50	I	EVCI	70	O	DIDT
11	O	PDO	31	O	ADSY	51	O	EVCO	71	I	DODT
12	–	GND	32	O	SQSY	52	–	GND	72	I	DOVF
13	O	EFMO	33	–	VDD	53	O	MCLK	73	–	VDD
14	O	ATER	34	O	DQSY	54	I	XTAI	74	I	TEST3
15	I	CNIN	35	O	TEST7	55	O	XTAO	75	O	TEST4
16	O	SENS	36	I	DTI	56	I	TEST9	76	I	TEST5
17	I	SYPL	37	O	DTO	57	I	MVCI	77	I	TEST6
18	O	FILO	38	O	C2PO	58	O	MVCO	78	I	FMCK
19	I	FILI	39	O	BCK	59	O	TEST2	79	I	FMDT
20	O	PCO	40	O	XBCK	60	O	DIPD	80	I	ADFG


PCO 20
FILI 19
FILO 18
CLTV 22
34MHz PLL
VCOI 9
VCOO 8
DECODE CLOCK GENERATOR
EFMI 5
EFM DEMODULATOR
ASY 6
PDO 11
XPLCK 46
DECODER PLL
GTOP 44
GFS 47
XUGFS 45
SYNC DET./INS.
TIMING GENREATOR
LOCK 7
FSW 1
MON 2
MDP 3
MDS 4
ADFG 80
CLV CONTROL
SENS CONTROL
CNIN 15
FMDT 79
FMCK 78
ATER 14
ADSY 31
ADIP DECODER
EFMO 13
EFM DEMODULATOR
EPDO 48
DECODER PLL
EVCI 50
EVCO 51
ENCODE CLOCK GENERATOR
REGISTOR
REGISTOR
BUS
RAM
AUDIO CONTROL
ECC ENCODER/ DECODER
TIMING GENERATOR
SUBQ READER/ GENERATOR
SUBQ PROCCESOR
CPU COMMAND I/F
27 SCLK
28 XLAT
29 SWDT
30 SRDT
24 XRST
25 REC
17 SYPL
37 DTO
36 DTI
61 RAOF
38 C2PO
62, 63, 64 MT0-3
CLOCK GENERATOR
54 XTAI
55 XTAO
57 MVCI
58 MVCO
39, 40 BCK. XBCK
42 WDCK
41 LRCK
53 MCLK
43 FS4
49 RFCK
16 SENS
66 WFCK
PEAK DETECT
68 MD2
71 DODT
72 DOVF
DIGITAL IN/OUT
69 DOUT
70 DIDT
67 DIN
34 DQSY
DIGITAL IN PLL
60 DIPD
32 SQSY


19 FILI
22 CLTV
9 VCOI
5 EFMI
80 ADFG
78 FMCK
79 FMDT
54 XTAI
57 MVCI
50 EVCI
68 MD2
71 DODT
72 DOVF
67 DIN
36 DTI
27 SCLK
28 XLAT
29 SWDT
17 SYPL
24 XRST
25 REC
15 CNIN
10 TEST1
74 TEST3
76 TEST5
77 TEST6
26 TEST8
56 TEST9
20 PCO
18 FILO
8 VCOO
6 ASY
11 PDO
46 XPLCK
44 GTOP
47 GFS
45 XUGFS
55 XTAO
58 MVCO
7 LOCK
1 FSW
2 MON
3 MDP
4 MDS
14 ATER
31 ADSY
39 BCK
40 XBCK
41 LRCK
42 WDCK
43 FS4
53 MCLK
49 RFCK
51 EVCO
48 EPDO
13 EFMO
69 DOUT
70 DIDT
34 DQSY
60 DIPD
32 SQSY
37 DTO
61 RAOF
38 C2PO
62 MT3
63 MT2
64 MT1
65 MT0
30 SRDT
66 WFCK
16 SENS
59 TEST2
75 TEST4
35 TEST7

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FSW   ;SPINDLE MOTOR OUTPUT FILTER SWITCHING OUTPUT
MON   ;SPINDLE MOTOR ON/OFF CONTROL OUTPUT, WHEN "H" :ON
MDP   ;SPINDLE MOTOR SERVO CONTROL
MDS   ;SPINDLE MOTOR SERVO CONTROL
EFMI  ;EFM INPUT WHEN PLAYBACK MODE
ASY   ;EFM FULL SWING OUTPUT WHEN PLAYBACK MODE
LOCK  ;SPINDLE SERVO (CLV) LOCKED STATE MONITOR, WHEN "H" :LOCKED
VCO0  ;EFM DECODER, ANALOG PLL OSCILLATION OUTPUT (196Fs=8.6436MHz)
VCO1  ;EFM DECODER, ANALOG PLL OSCILLATION INPUT
TEST1 ;TEST PIN (NORMALLY SET TO GROUND)
PDO   ;EFM DECODER, ANALOG PLL PHASE COMPARISON OUTPUT
EFMO  ;EFM OUTPUT WHEN REC MODE
ATER  ;ADIP CRC FLAG OUTPUT, WHEN "H" :ERROR
CNIN  ;TRACK JUMP NUMBER COUNT SIGNAL INPUT
SENS  ;INTERNAL STATUS OUTPUT
SYPL  ;POLARITY SWITCHING INPUT PIN OF SQSY, ADSY, AND DQSY
FIFO  ;MASTER PLL FILTER OUTPUT FOR DIGITAL PLL
FILI  ;MASTER PLL FILTER INPUT FOR DIGITAL PLL
PCO   ;MASTER PLL PHASE COMPARISON OUTPUT FOR DIGITAL PLL
CLTV  ;MASTER PLL VCO CONTROL VOLTAGE INPUT FOR DIGITAL PLL
XRST  ;SYSTEM RESET INPUT (ACTIVE LOW)
REC   ;WHEN "L" :DECODER, "H"   :ENCODER
TEST8 ;TEST PIN (NORMALLY SET TO GROUND)
SCLK  ;SERIAL BUS CLOCK INPUT
XLAT  ;SERIAL BUS LATCH INPUT
SWDT  ;SERIAL BUS WRITE DATA INPUT
SRDT  ;SERIAL BUS READ OUT DATA OUTPUT
ADSY  ;ADIP SYNC OUTPUT
SQSY  ;SUBCODE Q SYNC OUTPUT
DQSY  ;SUBCODE Q SYNC (SCOR) OUTPUT OF DIGITAL IN U-BIT CD FORMAT
TEST7 ;SET TO  "OPEN"
DT1   ;RECORDING AUDIO SIGNAL INPUT
DT0   ;PLAYBACK AUDIO SIGNAL OUTPUT, (REC MODE;HIGH-IMPEDANCE)
C2PO  ;SET TO C2PO WHEN PLAYBACK, D.IN-VFLAG WHEN D.REC, A.REC
       WHEN "0" .
BCK   ;2.8224MHz OUTPUT (MCLK SYSTEM)
XBCK  ;BCK INVERSION OUTPUT (MCLK SYSTEM)
LRCK  ;44.1kHz (=Fs) (MCLK SYSTEM)
WDCK  ;88.2kHz (MCLK SYSTEM)
FS4   ;176.4kHz (MCLK SYSTEM)
GTOP  ;WHEN "H" :SYNC GUARD WINDOW OPENS (INPUT EFM SYNC MONITOR OUTPUT)
XUGFS ;WHEN "L" :UNGUARDED FRAME SYNC (INPUT EFM SYNC MONITOR OUTPUT)
XPLCK ;EFM DECODER PLL CLOCK OUTPUT (98Fs=4.3218MHz)
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GFS ;WHEN "H" :FRAME SYNC OK(INPUT EFM SYNC MONITOR OUTPUT)
EPDO ;EFM ENCODER EXTERNAL PLL PHASE COMPARISON OUTPUT
RFCK ;7.35kHzOUTPUT(MCLK SYSTEM)
EVC1 ;EFM ENCODER EXTERNAL PLL OSCILLATION INPUT(196Fs=8.6436MHz)
EVC0 ;EFM ENCODER OUTSIDE PLL OSCILLATION OUTPUT(196Fs=8.6436MHz)
MCLK ;22.5792MHzOUTPUT
XTAI ;CRYSTAL OSCILLATION INPUT(512Fs=22.5792MHz)
XTAO ;CRYSTAL OSCILLATION OUTPUT(512Fs=22.5792MHz)
MVCI ;DIGITAL IN PLL OSCILLATION INPUT(512Fs=22.5792MHz)
MVCO ;DIGITAL IN PLL OSCILLATION OUTPUT(512Fs=22.5792MHz)
DIPD ;DIGITAL IN PLL PHASE COMPARISON OUTPUT
RAOF ;RAM OVERFLOW OUTPUT(DECODER MONITOR OUTPUT)
MT0-3 ;CORRECTING STATE MONITOR OUTPUT
WFCK ;7.35kHzOUTPUT.(SET TO EFM DECODER PLL SYSTEM WHEN
PLAYBACK,EFM DECODER PLL SYSTEM WHEN RECORDING.)
DIN ;DIGITAL AUDIO INPUT
MD2 ;DIGITAL AUDIO OUTPUT ON/OFF ("H" :ON)
DOUT ;DIGITAL AUDIO OUTPUT
DIDT ;AUDIO DATA OUTPUT OF DIGITAL AUDIO INPUT
DODT ;16-BIT DATA INPUT FOR DIGITAL AUDIO OUTPUT
DOVF ;VALIDITY FLAG INPUT FOR DIGITAL AUDIO OUTPUT
TEST9,3,5,6 ;FIXED TO "L"
TEST2,4,7 ;SET TO "OPEN"
FMCK ;ADIP READ OUT CLOCK INPUT(6.3kHz)
FMDT ;ADIP DATA INPUT
ADFG ;ADIP CARRIER SIGNAL INPUT