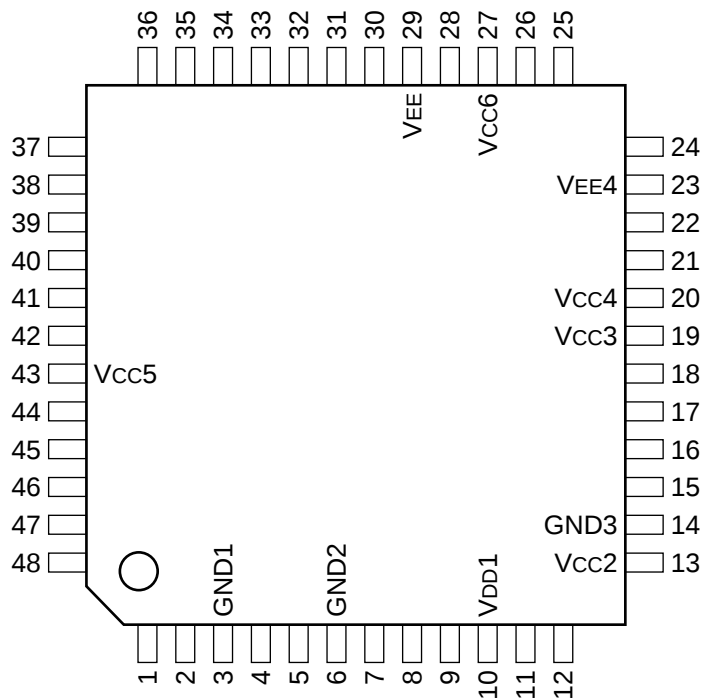


TIMING GENERATOR WITH CCD ELECTRICAL IMAGE STABILIZER CONTROL
—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	CLPDM	13	—	Vcc2	25	O	V2	37	I	SSK
2	O	PBLK	14	—	GND3	26	O	V1	38	I	SSI
3	—	GND1	15	O	XSHP	27	—	Vcc6	39	I	SEN
4	I	OSCI	16	O	XSHD	28	O	V3	40	I	RST
5	O	OSCO	17	O	XRS	29	—	VEE	41	I/O	XV1
6	—	GND2	18	O	RG	30	—	GND	42	I	DSGAT
7	I	CK	19	—	Vcc3	31	O	V4	43	—	Vcc5
8	I	TESTEN	20	—	Vcc4	32	I/O	XSG1	44	I	AHD
9	O	CCDCKL	21	O	H1	33	I	VSK	45	I	AVD
10	—	Vdd1	22	O	H2	34	I	VSI	46	—	CKINH
11	O	CCDCKH	23	—	VEE4	35	I	VEN	47	O	WEN
12	O	VICK	24	O	SUB	36	I	VGAT	48	O	ID

INPUT

AHD : HORIZONTAL DRIVE
 AVD : VERTICAL DRIVE
 CK : CLOCK (NTSC : 1820fH, PAL : 1816fH)
 DSGAT : SAMPLE HOLD PULSE GENERATOR CONTROL
 OSCI : OSCILLATOR (NTSC : 1820fH, PAL : 1816fH)
 RST : RESET
 SEN : MODE SERIAL INTERFACE STROBE
 SSI : MODE SERIAL INTERFACE DATA
 SSK : MODE SERIAL INTERFACE CLOCK
 TESTEN : IC TEST CONTROL
 VEN : VERTICAL SERIAL INTERFACE STROBE
 VGAT : CLOCK PULSE WAVEFORM CONTROL
 VSI : VERTICAL SERIAL INTERFACE DATA
 VSK : VERTICAL SERIAL INTERFACE CLOCK

OUTPUT

CCDCKH : MASTER CLOCK FOR 510H
 NTSC/510H : $(606+2/3)$ fH
 PAL/510H : $(605+1/3)$ fH
 CCDCKL : MASTER CLOCK FOR 760H
 NTSC/760H : 910fH
 PAL/760H : 908fH
 CLPDM : CCD DUMMY SIGNAL CLAMP
 H1, H2 : HORIZONTAL REGISTER CLOCK
 ID : VERTICAL LINE DISCRIMINATION
 MCK : MASTER CLOCK
 OSCO : OSCILLATOR (NTSC : 1820fH, PAL : 1816fH)
 PBLK : PRE-BLANKING PULSE
 RG : RESET GATE PULSE
 SUB : SHUTTER PULSE
 V1 - V4 : VERTICAL REGISTER CLOCK
 VICK : VIDEO FREE RUN CLOCK
 VSHP : SAMPLE HOLD PULSE (NTSC : 910fH, PAL : 908fH)
 WEN : MEMORY WRITE TIMING
 XRS : PHASE ADJUST SAMPLE HOLD PULSE
 XSG2 : SENSOR READ CLOCK
 XSHD : DATA LEVEL SAMPLE HOLD PULSE
 XSHP : PRE-CHARGE LEVEL SAMPLE HOLD PULSE

INPUT/OUTPUT

XSG1 : SENSOR READ CLOCK
 XV1 : VERTICAL REGISTER CLOCK

