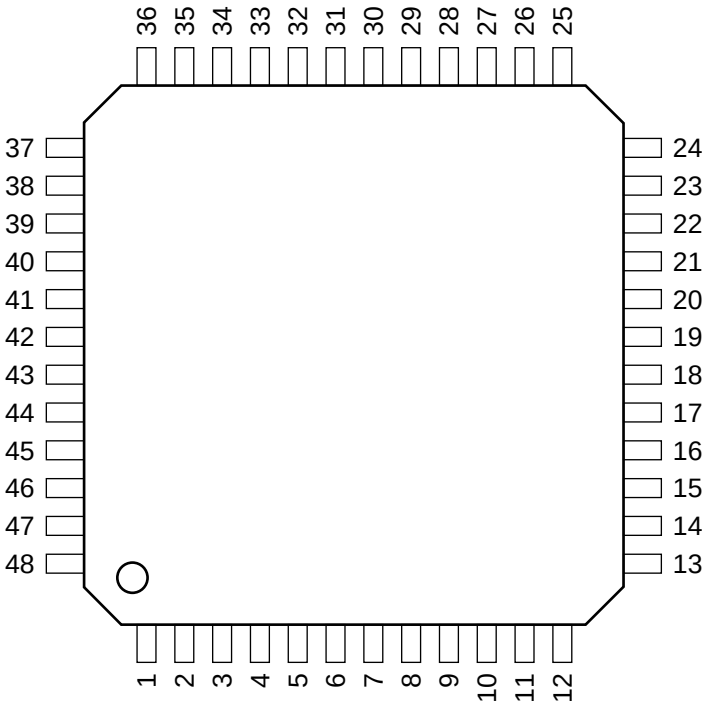
TIMING GENERATOR FOR CCD IMAGE SENSOR

—TOP VIEW—



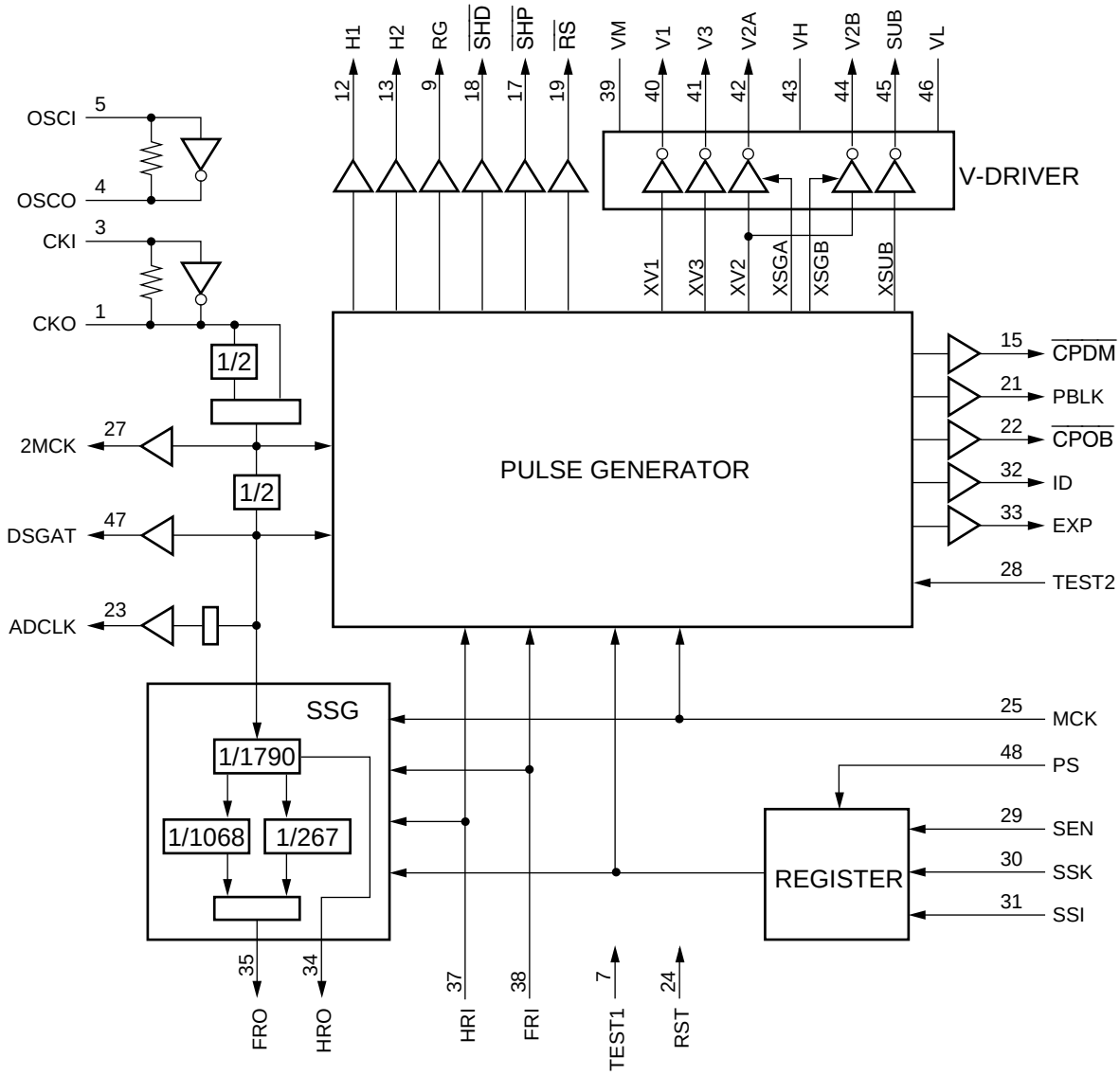
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	CKO	13	O	H2	25	O	MCK	37	I	HRI
2	—	V_{EE}	14	—	V_{CC}	26	—	V_{CC}	38	I	FRI
3	I	CKI	15	O	$\overline{CPDM}$	27	O	2MCK	39	—	VM
4	O	OSCO	16	—	V_{CC}	28	I	TEST2	40	O	V1
5	I	OSCI	17	O	$\overline{SHP}$	29	I	SEN	41	O	V3
6	—	V_{CC}	18	O	$\overline{SHD}$	30	I	SSK	42	O	V2A
7	I	TEST1	19	O	$\overline{RS}$	31	I	SSI	43	—	VH
8	—	V_{CC}	20	—	V_{EE}	32	O	ID	44	O	V2B
9	O	RG	21	O	PBLK	33	O	EXP	45	O	SUB
10	—	V_{EE}	22	O	$\overline{CPOB}$	34	O	HRO	46	—	VL
11	—	V_{EE}	23	O	ADCLK	35	O	FRO	47	I	DSGAT
12	O	H1	24	I	RST	36	—	V_{EE}	48	I	PS

INPUTS

CKI	:	OSCILLATOR (28.636 MHz)
DSGAT	:	OUTPUT DISABLE
FRI	:	V SYNC
HRI	:	H SYNC
OSCI	:	OSCILLATOR INVERTER
PS	:	PARALLEL/SERIAL SELECT
RST	:	RESET
SEN	:	DRIVE FREQ. SETTING/SERIAL STROBE
SSI	:	SHUTTER SPEED SETTING/SERIAL DATA
SSK	:	READ SETTING/SERIAL CLOCK
TEST1, TEST2	:	(FOR TEST)

OUTPUTS

2MCK	:	X2 MASTER CLOCK
ADCLK	:	A/D CONVERTER CLOCK
CKO	:	OSCILLATOR (28.636 MHz)
$\overline{\text{CPDM}}$	:	CLAMP PULSE
$\overline{\text{CPOB}}$	:	CLAMP PULSE
EXP	:	EXPOSURE PULSE
FRO	:	V SYNC
H1, H2	:	H CCD DRIVE CLOCK
HRO	:	H SYNC
ID	:	LINE ID WRITE ENABLE PULSE
MCK	:	MASTER CLOCK
OSCO	:	OSCILLATOR INVERTER
PBLK	:	BLANKING CLEANING PULSE
RG	:	RESET GATE PULSE
$\overline{\text{RS}}$	:	SAMPLE/HOLD PULSE
$\overline{\text{SHD}}$	:	SAMPLE/HOLD PULSE
$\overline{\text{SHP}}$	:	SAMPLE/HOLD PULSE
SUB	:	CCD SUBSTRATE PULSE
V1, V2A, V2B, V3	:	V CCD DRIVE CLOCK


H1
H2
RG
SHD
SHP
RS
VM
V1
V3
V2A
VH
V2B
SUB
VL
12
13
9
18
17
19
39
40
41
42
43
44
45
46
V-DRIVER
XV1
XV3
XV2
XSGA
XSGB
XSUB
OSCI
5
OSCO
4
CKI
3
CKO
1
1/2
1/2
2MCK
27
DSGAT
47
ADCLK
23
PULSE GENERATOR
15
CPDM
21
PBLK
22
CPOB
32
ID
33
EXP
28
TEST2
SSG
1/1790
1/1068
1/267
25
MCK
48
PS
29
SEN
30
SSK
31
SSI
REGISTER
35
34
37
38
7
24
FRO
HRO
HRI
FRI
TEST1
RST