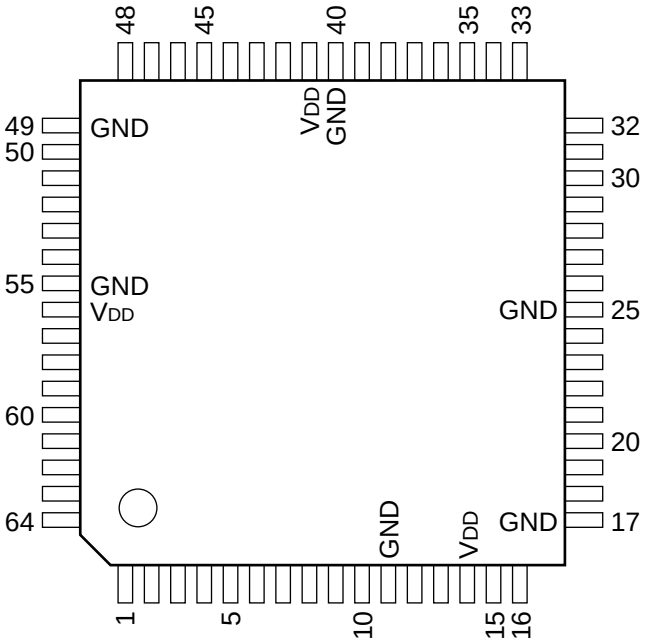
C-MOS TIMING GENERATOR FOR PROGRESSIVE SCAN READOUT SYSTEM CCD IMAGE SENSOR

-TOP VIEW-



(VDD = +5V)

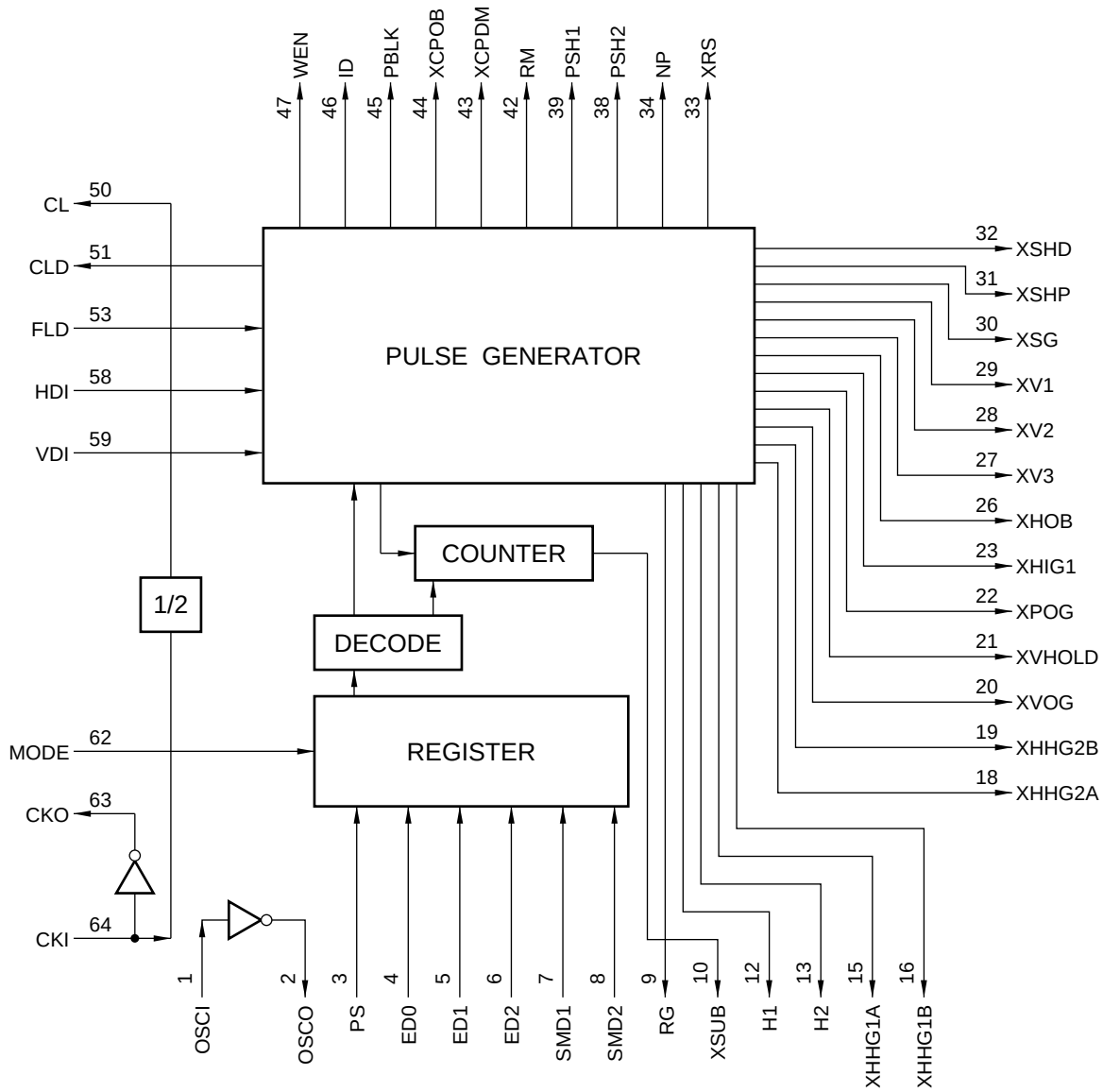
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	OSCI	17	—	GND	33	O	XRS	49	—	GND
2	O	OSCO	18	O	XHHG2A	34	I	NP	50	O	CL
3	I	PS	19	O	XHHG2B	35	I	TEST1	51	O	CLD
4	I	ED0	20	O	XVOG	36	I	TEST2	52	I	TEST5
5	I	ED1	21	O	XVHOLD	37	I	TEST3	53	O	FLD
6	I	ED2	22	O	XPOG	38	O	PSH2	54	I	TEST6
7	I	SMD1	23	O	XHIG1	39	O	PSH1	55	—	GND
8	I	SMD2	24	—	VDD	40	—	GND	56	—	VDD
9	O	RG	25	—	GND	41	—	VDD	57	I	TEST7
10	O	XSUB	26	O	XHOB	42	I	RM	58	I	HDI
11	—	GND	27	O	XV3	43	O	XCPDM	59	I	VDI
12	O	H1	28	O	XV2	44	O	XCPOB	60	I	TEST8
13	O	H2	29	O	XV1	45	O	PBLK	61	I	TEST9
14	—	VDD	30	O	XSG	46	O	ID	62	I	MODE
15	O	XHHG1A	31	O	XSHP	47	O	WEN	63	O	CKO
16	O	XHHG1B	32	O	XSHD	48	I	TEST4	64	I	CKI

INPUT

CKI	; 2fCK CLOCK
ED0 - ED2	; SHUTTER SPEED SETTING
HDI	; HORIZONTAL SYNC
MODE	; READ MODE SELECT (L: 2ch H: 1ch)
NP	; NTSC/PAL MODE SELECT (L: NTSC H: PAL)
OSCI	; OSCILLATOR INVERTER
PS	; ELECTRON SHUTTER SPEED INPUT SWITCH
RM	; MODE SELECT (L: INTERLACE H: NONINTERLACE)
SMD1, SMD2	; SHUTTER MODE SETTING
TEST1 - TEST4, TEST6 - TEST9	; TEST
VDI	; VERTICAL SYNC

OUTPUT

CKO	; 2fCK CLOCK
CL	; fCK CLOCK (0°)
CLD	; fCK CLOCK (90°)
FLD	; FIELD SIGNAL
H1, H2	; DRIVE PULSE (CCD HORIZONTAL REGISTER)
HDO	; HORIZONTAL SYNC
ID	; LINE DETECT
OSCO	; OSCILLATOR INVERTER
PBLK	; BLANKING CLEANING PULSE
PSH1, PSH2	; REFERENCE SIGNAL SAMPLE HOLD PULSE
RG	; RESET GATE PULSE
TEST5	; TEST
WEN	; WRITE ENABLE
XCPDM	; CLAMP PULSE
XCPOB	; CLAMP PULSE
XHHG1A, XHHG1B	; TRANSFER CLOCK (CCD HORIZONTAL REGISTER DURING)
XHHG2A, XHHG2B	; TRANSFER CLOCK (CCD HORIZONTAL REGISTER DURING)
XHIG1	; DRIVE CLOCK (REFERENCE SIGNAL INJECTION GATE)
XHOB	; DRIVE CLOCK (DRAIN GATE)
XPOG	; TRANSFER (REFERENCE SIGNAL HORIZONTAL REGISTER)
XRS	; SAMPLE HOLD PULSE
XSG	; CCD SENSOR ELECTRIC READ OUT PULSE
XSHD	; DATA SAMPLE HOLD PULSE
XSHP	; SAMPLE HOLD PULSE (PRE-CHARGE LEVEL)
XSUB	; CCD ELECTRIC SWEEP THROW AWAY
XV1 - XV3	; DRIVE CLOCK (CCD VERTICAL REGISTER)
XVHOLD	; ADJUST CLOCK (CCD HORIZONTAL REGISTER TRANSFER TIMMING)
XVOG	; TRANSFER CLOCK (CCD VERTICAL REGISTER → CCD HORIZONTAL REGISTER)


PULSE GENERATOR
COUNTER
DECODE
REGISTER
1/2
CL
CLD
FLD
HDI
VDI
MODE
CKO
CKI
OSCI
OSCO
WEN
ID
PBLK
XCPOB
XCPDM
RM
PSH1
PSH2
NP
XRS
PS
ED0
ED1
ED2
SMD1
SMD2
RG
XSUB
H1
H2
XHHG1A
XHHG1B
XSHD
XSHP
XSG
XV1
XV2
XV3
XHOB
XHIG1
XPOG
XVHOLD
XVOG
XHHG2B
XHHG2A