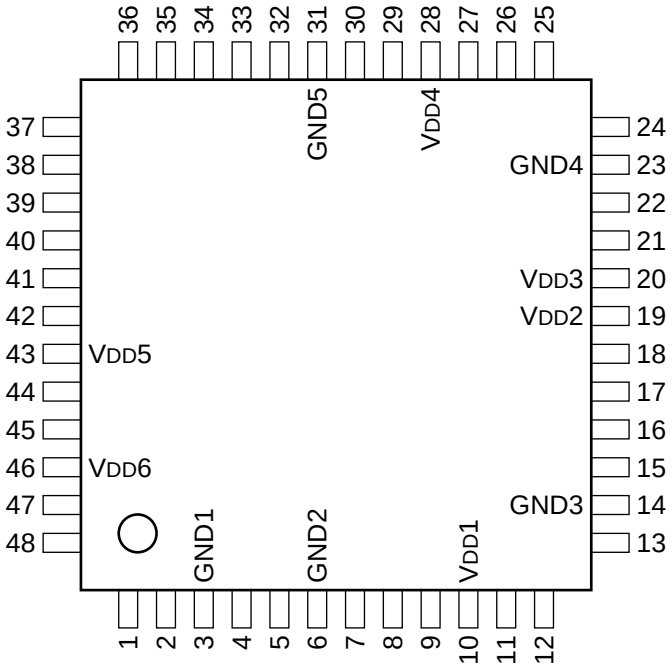
C-MOS TIMING GENERATOR WITH CCD ELECTRICAL IMAGE STABILIZER CONTROL

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	CDLPDM	13	O	NON	25	O	XV2	37	I	SSK
2	O	PBLK	14	—	GND3	26	O	XV1	38	I	SSI
3	—	GND1	15	O	XSHP	27	O	XSG1	39	I	SEN
4	I	OSCI	16	O	XSHD	28	—	$V_{DD}4$	40	I	RST
5	O	OSCO	17	O	XRS	29	O	XV3	41	I	TEST2
6	—	GND2	18	O	RG	30	O	XSG2	42	I	DSGAT
7	I	CK	19	—	$V_{DD}2$	31	—	GND5	43	—	$V_{DD}5$
8	I	TEST1	20	—	$V_{DD}3$	32	O	XV4	44	I	AHD
9	O	MCK	21	O	H1	33	I	VSK	45	I	AVD
10	—	$V_{DD}1$	22	O	H2	34	I	VSI	46	—	$V_{DD}6$
11	O	VSHP	23	I	GND4	35	I	VEN	47	O	WEN
12	O	CL	24	O	XSUB	36	I	VGAT	48	O	ID

INPUT

AHD : HORIZONTAL DRIVE
AVD : VERTICAL DRIVE
CK : CLOCK (NTSC : 1820fH, PAL : 1816fH)
DSGAT : SAMPLE HOLD PULSE GENERATOR CONTROL
OSCI : OSCILLATOR (NTSC : 1820fH, PAL : 1816fH)
RST : RESET
SEN : MODE SERIAL INTERFACE STROBE
SSI : MODE SERIAL INTERFACE DATA
SSK : MODE SERIAL INTERFACE CLOCK
TEST1 : TEST
TEST2 : TEST
VEN : VERTICAL SERIAL INTERFACE STROBE
VGAT : CLOCK PULSE WAVEFORM CONTROL
VSI : VERTICAL SERIAL INTERFACE DATA
VSK : VERTICAL SERIAL INTERFACE CLOCK

OUTPUT

CL : CLOCK
CLPDM : CCD DUMMY SIGNAL CLAMP
H1 : HORIZONTAL REGISTER CLOCK
H2 : HORIZONTAL REGISTER CLOCK
ID : VERTICAL LINE DISCRIMINATION
MCK : MASTER CLOCK
  NTSC/510H : (606+2/3)fH
  NTSC/760H : 910fH
  PAL/510H : (605+1/3)fH
  PAL/760H : 908fH
  VTR MODE(NTSC) : 910fH
  VTR MODE(PAL) : 908fH
OSCO : OSCILLATOR (NTSC : 1820fH, PAL : 1816fH)
PBLK : PRE-BLANKING PULSE
RG : RESET GATE PULSE
VSHP : SAMPLE HOLD PULSE (NTSC : 910fH, PAL : 908fH)
WEN : MEMORY WRITE TIMING
XRS : PHASE ADJUST SAMPLE HOLD PULSE
XSG1 : SENSOR READ CLOCK
XSG2 ; SENSOR READ CLOCK
XSHD : DATA LEVEL SAMPLE HOLD PULSE
XSHP : PRE-CHARGE LEVEL SAMPLE HOLD PULSE
XSUB : SHUTTER PULSE
XV1 : VERTICAL REGISTER CLOCK
XV2 : VERTICAL REGISTER CLOCK
XV3 : VERTICAL REGISTER CLOCK
XV4 : VERTICAL REGISTER CLOCK