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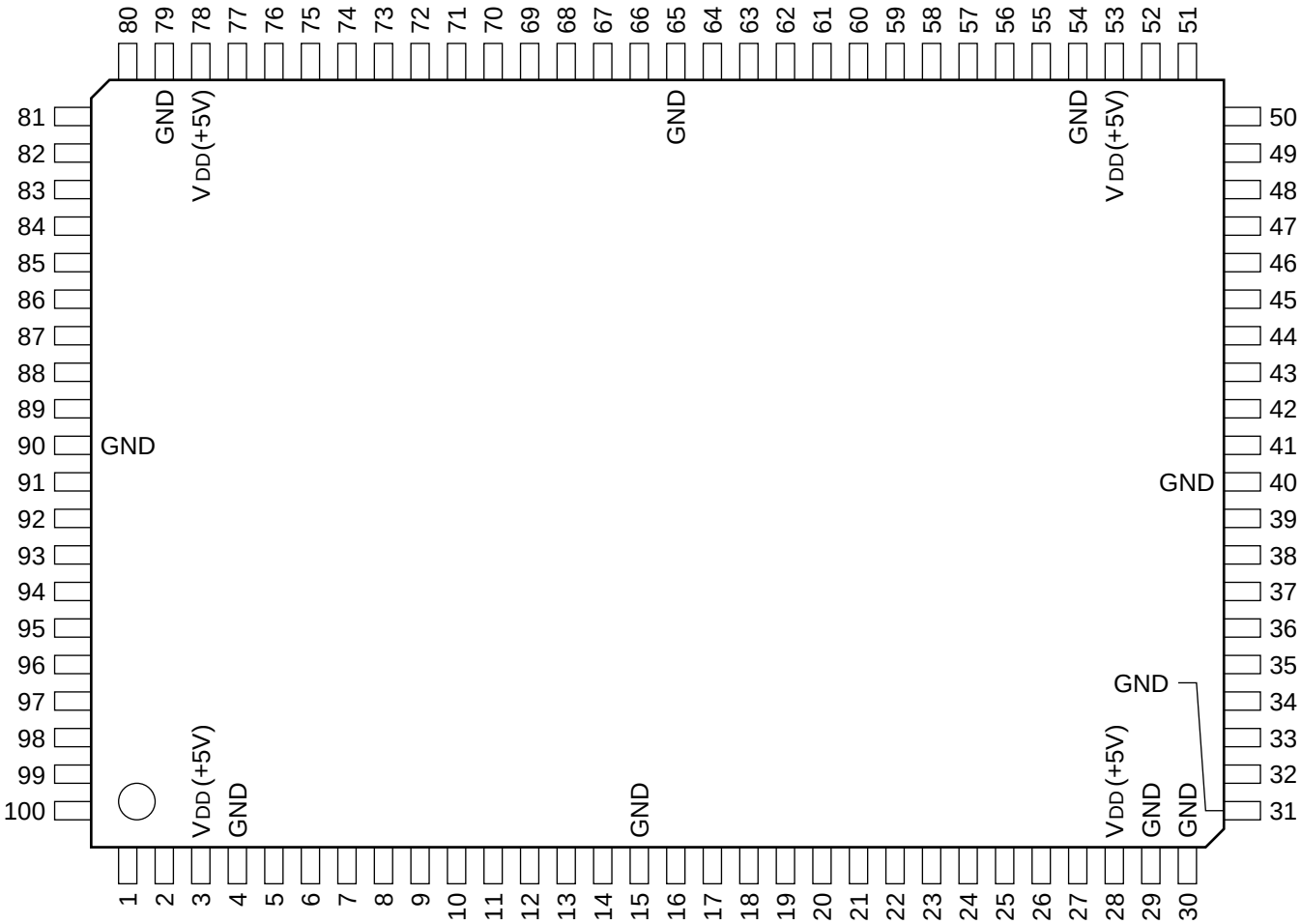
IL08

C-MOS DOUBLE-SPEED SCAN CONVERTER

- TOP VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	DMP-CLK	26	O	CD4	51	O	H-PHASE	76	I	YSD5
2	I	DMP-ID	27	O	CD3	52	I	CSD0	77	I	YSD6
3	–	V_{DD}	28	–	V_{DD}	53	–	V_{DD}	78	–	V_{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	I	DMP-MOSI	30	O	CD2	55	I	CSD1	80	I	YSD7
6	O	DMP-MISO	31	O	CD1	56	I	CSD2	81	I	YFD0
7	I/O	P0	32	O	CD0	57	I	CSD3	82	I	YFD1
8	I/O	P1	33	O	YD7	58	I	CSD4	83	I	YFD2
9	I/O	P2	34	O	YD6	59	I	CSD5	84	I	YFD3
10	O	OVBLK	35	O	YD5	60	I	CSD6	85	I	YFD4
11	I	PRE-SW	36	O	YD4	61	I	CSD7	86	I	YFD5
12	I	HSW-SW	37	O	YD3	62	I	CFD0	87	I	YFD6
13	I	LDSP-SW	38	O	YD2	63	I	CFD1	88	I	YFD7
14	I	YDL-SW	39	O	YD1	64	I	CFD2	89	O	WLRS2
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	I	BLNK	41	O	YD0	66	I	CFD3	91	O	WRS2
17	I	SIO-SEL	42	O	B-YD/A	67	I	CFD4	92	O	WEN2
18	I	TEST	43	O	R-YD/A	68	I	CFD5	93	O	WLRS1
19	I	MRST	44	I	YD/A	69	I	CFD6	94	O	WRS1
20	O	VD-OUT	45	I	EXRDCK	70	I	CFD7	95	O	WEN1
21	O	HD-OUT	46	O	REN1/2	71	I	YSD0	96	I	H-IN
22	O	OHBLK	47	O	RRS1	72	I	YSD1	97	I	V-IN
23	O	CD7	48	O	RRS2	73	I	YSD2	98	I	EXINCK
24	O	CD6	49	O	RLRS1/2	74	I	YSD3	99	O	B-YOE
25	O	CD5	50	O	V-PHASE	75	I	YSD4	100	O	R-YOE

INPUT

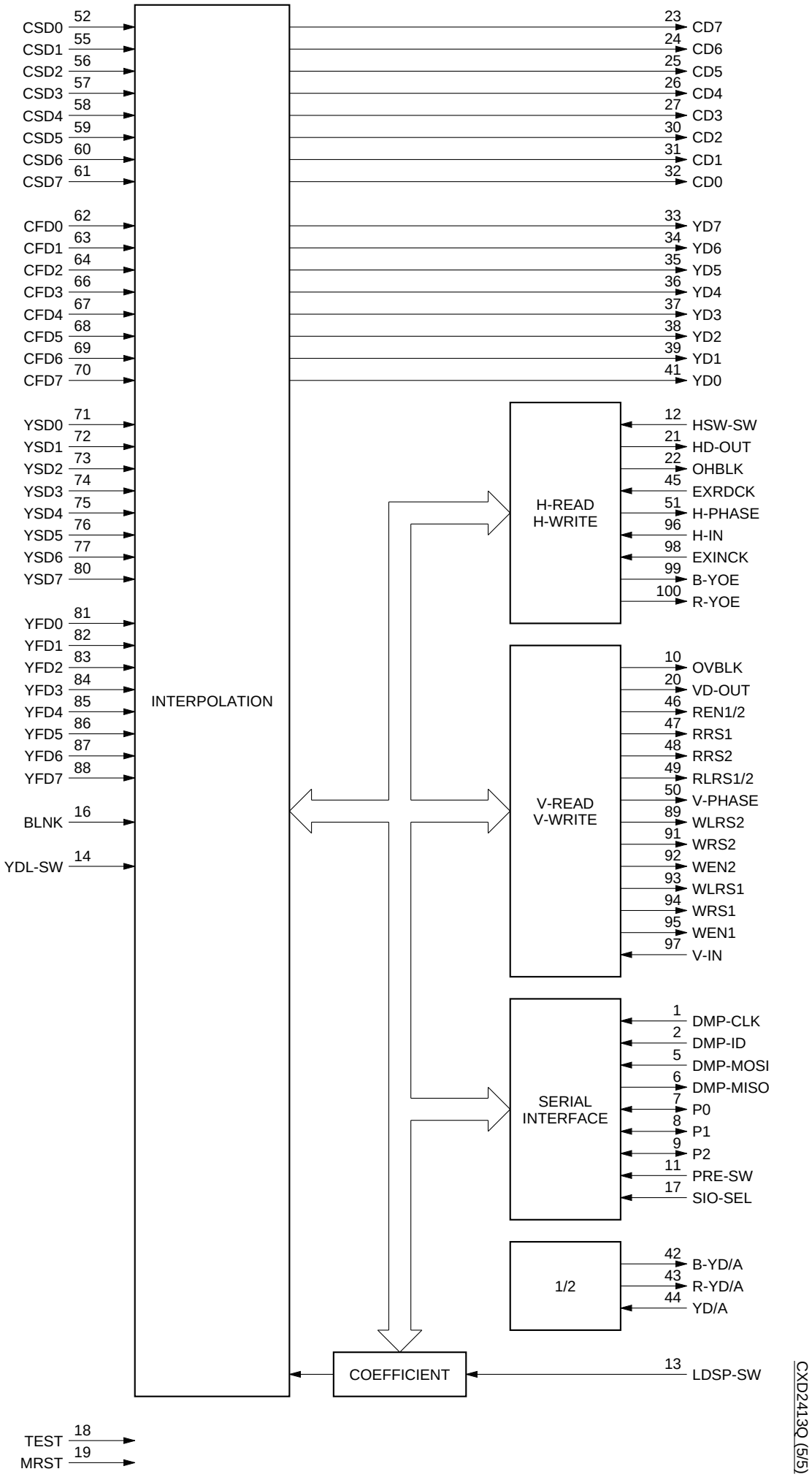
BLNK	; OUTPUT VIDEO BLANKING SIGNAL
CFD0-CFD7	; R-Y/B-Y FIRST LINE SIGNAL
CSD0-CSD7	; R-Y/B-Y SECOND LINE SIGNAL
DMP-CLK	; SERIAL CLOCK
DMP-ID	; SERIAL CONTROL
DMP-MOSI	; SERIAL DATA
EXINCK	; WRITE CLOCK
EXRDCK	; READ CLOCK
H-IN	; H SYNCHRONIZING SIGNAL
HSW-SW	; H SYNCHRONIZING SIGNAL OUTPUT WIDTH SETTING
LDSP-SW	; LINE DISPLAY OF DEMARCATION BETWEEN VIDEO AND CAPTION
MRST	; RESET (H FIXED)
PRE-SW	; PORT PRESET
SIO-SEL	; SERIAL COMMUNICATION MODE SELECT
TEST	; TEST (L FEXED)
V-IN	; V SYNCHRONIZING SIGNAL
YD/A	; Y SIGNAL D/A CONVERTER CLOCK
YDL-SW	; Y SIGNAL OUTPUT DELAY SETTING
YFD0-YFD7	; Y FIRST LINE SIGNAL
YSD0-YSD7	; Y SECOND LINE SIGNAL

OUTPUT

B-YD/A	; B-Y SIGNAL D/A CONVERTER CLOCK
B-YOE	; B-Y SIGNAL OUTPUT ENABLE
CD0	; R-Y/B-Y SIGNAL
CD1-CD2	; GND
CD3-CD7	; R-Y/B-Y SIGNAL
DMP-MISO	; SERIAL DATA
H-PHASE	; H READ START PULSE
HD-OUT	; H SYNCHRONIZING SIGNAL
OHBLK	; H BLANKING
OVBLK	; V BLANKING
R-YD/A	; R-Y SIGNAL D/A CONVERTER CLOCK
R-YOE	; R-Y SIGNAL OUTPUT ENABLE
REN1/2	; FIELD MEMORY PORT 1/2 READ ENABLE
RLRS1/2	; FIELD MEMORY PORT 1/2 READ LINE RESET
RRS1	; FIELD MEMORY PORT 1 READ RESET
RRS2	; FIELD MEMORY PORT 2 READ RESET
VD-OUT	; V SYNCHRONIZING SIGNAL
V-PHASE	; V READ START PULSE
WEN1	; FIELD MEMORY PORT 1 WRITE ENABLE
WEN2	; FIELD MEMORY PORT 2 WRITE ENABLE
WLRS1	; FIELD MEMORY PORT 1 WRITE LINE RESET
WLRS2	; FIELD MEMORY PORT 2 WRITE LINE RESET
WRS1	; FIELD MEMORY PORT 1 WRITE RESET
WRS2	; FIELD MEMORY PORT 2 WRITE RESET
YD0-YD7	; Y SIGNAL

INPUT/OUTPUT

P0-P2	; I/O PORT


CSD0 52
CSD1 55
CSD2 56
CSD3 57
CSD4 58
CSD5 59
CSD6 60
CSD7 61
CFD0 62
CFD1 63
CFD2 64
CFD3 66
CFD4 67
CFD5 68
CFD6 69
CFD7 70
YSD0 71
YSD1 72
YSD2 73
YSD3 74
YSD4 75
YSD5 76
YSD6 77
YSD7 80
YFD0 81
YFD1 82
YFD2 83
YFD3 84
YFD4 85
YFD5 86
YFD6 87
YFD7 88
BLNK 16
YDL-SW 14
TEST 18
MRST 19
INTERPOLATION
23 CD7
24 CD6
25 CD5
26 CD4
27 CD3
30 CD2
31 CD1
32 CD0
33 YD7
34 YD6
35 YD5
36 YD4
37 YD3
38 YD2
39 YD1
41 YD0
H-READ
H-WRITE
12 HSW-SW
21 HD-OUT
22 OHBLK
45 EXRDCK
51 H-PHASE
96 H-IN
98 EXINCK
99 B-YOE
100 R-YOE
V-READ
V-WRITE
10 OVBLK
20 VD-OUT
46 REN1/2
47 RRS1
48 RRS2
49 RLRS1/2
50 V-PHASE
89 WLRS2
91 WRS2
92 WEN2
93 WLRS1
94 WRS1
95 WEN1
97 V-IN
SERIAL
INTERFACE
1 DMP-CLK
2 DMP-ID
5 DMP-MOSI
6 DMP-MISO
7 P0
8 P1
9 P2
11 PRE-SW
17 SIO-SEL
1/2
42 B-YD/A
43 R-YD/A
44 YD/A
COEFFICIENT
13 LDSP-SW

CXD2413Q (5/5)