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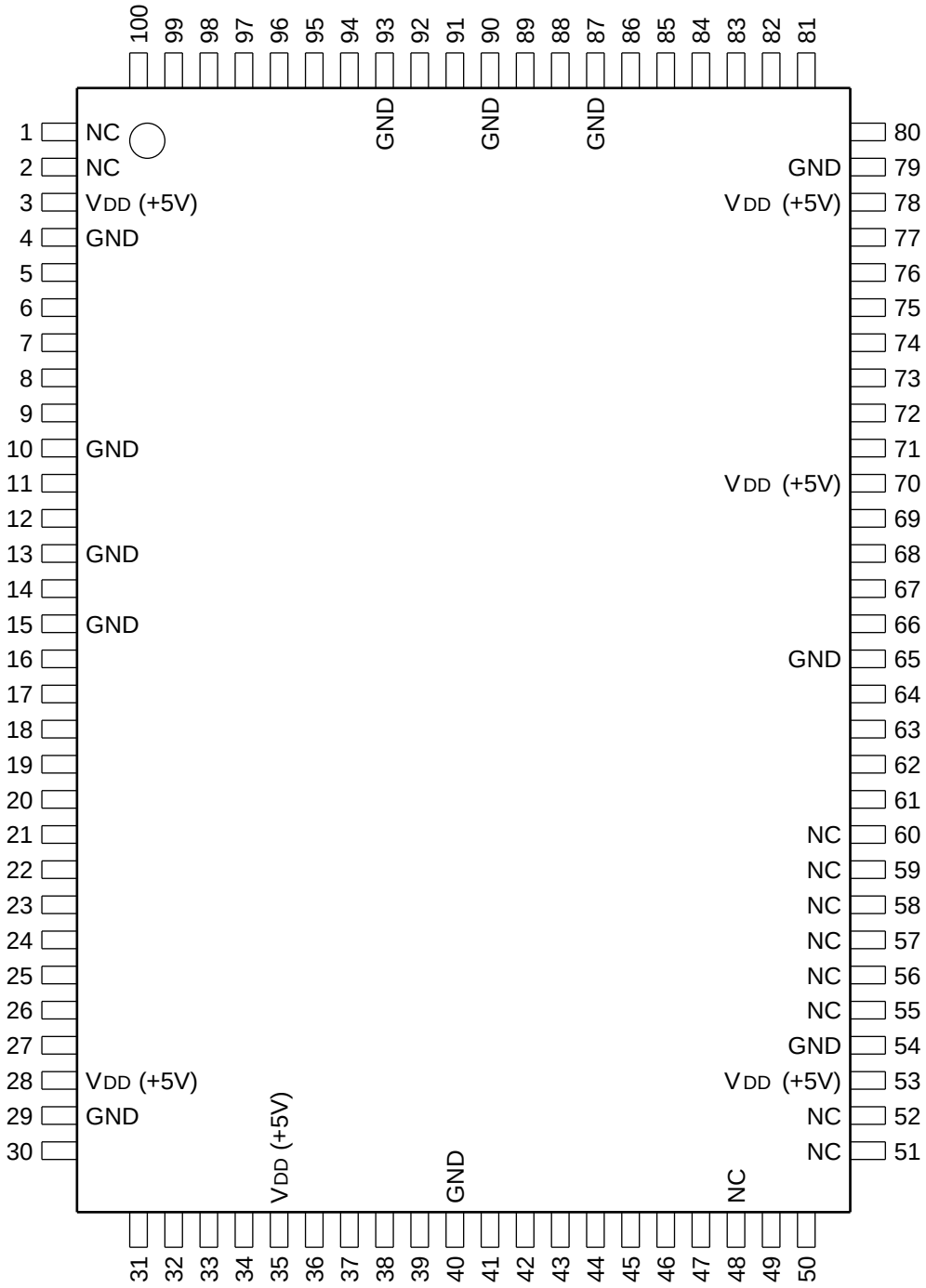
IL08

C-MOS TIMING GENERATOR FOR LCD PANEL

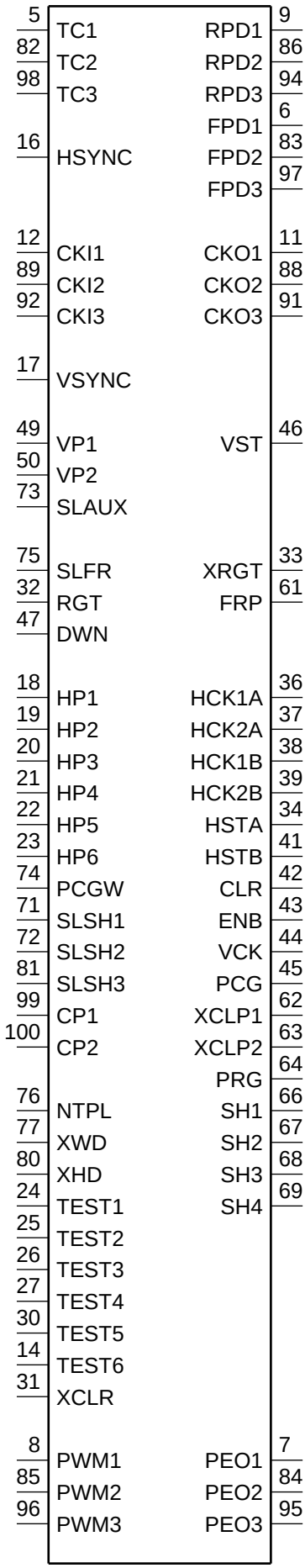
- TOP VIEW -



(V_{DD}=+5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	–	NC	26	I	TST3	51	–	NC	76	I	NTPL
2	–	NC	27	I	TST4	52	–	NC	77	I	XWD
3	–	V_{DD}	28	–	V_{DD}	53	–	V_{DD}	78	–	V_{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	I	TC1	30	I	TST5	55	–	NC	80	I	XHD
6	O	FPD1	31	I	XCLR	56	–	NC	81	I	SLSH3
7	O	PEO1	32	I	RGT	57	–	NC	82	I	TC2
8	I	PWM1	33	O	XRGT	58	–	NC	83	O	FPD2
9	O	RPD1	34	O	HSTA	59	–	NC	84	O	PEO2
10	–	GND	35	–	V_{DD}	60	–	NC	85	I	PWM2
11	O	CKO1	36	O	HCK1A	61	O	FRP	86	O	RPD2
12	I	CKI1	37	O	HCK2A	62	O	XCLP1	87	–	GND
13	–	GND	38	O	HCK1B	63	O	XCLP2	88	O	CKO2
14	I	TST6	39	O	HCK2B	64	O	PRG	89	I	CKI2
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	I	HSYNC	41	O	HSTB	66	O	SH1	91	O	CKO3
17	I	VSYNC	42	O	CLR	67	O	SH2	92	I	CKI3
18	I	HP1	43	O	ENB	68	O	SH3	93	–	GND
19	I	HP2	44	O	VCK	69	O	SH4	94	O	RPD3
20	I	HP3	45	O	PCG	70	–	V_{DD}	95	O	PEO3
21	I	HP4	46	O	VST	71	I	SLSH1	96	I	PWM3
22	I	HP5	47	I	DWN	72	I	SLSH2	97	O	FPD3
23	I	HP6	48	–	NC	73	I	SLAUX	98	I	TC3
24	I	TST1	49	I	VP1	74	I	PCGW	99	I	CP1
25	I	TST2	50	I	VP2	75	I	SLFR	100	I	CP2

CXD2412AQ (3/6)

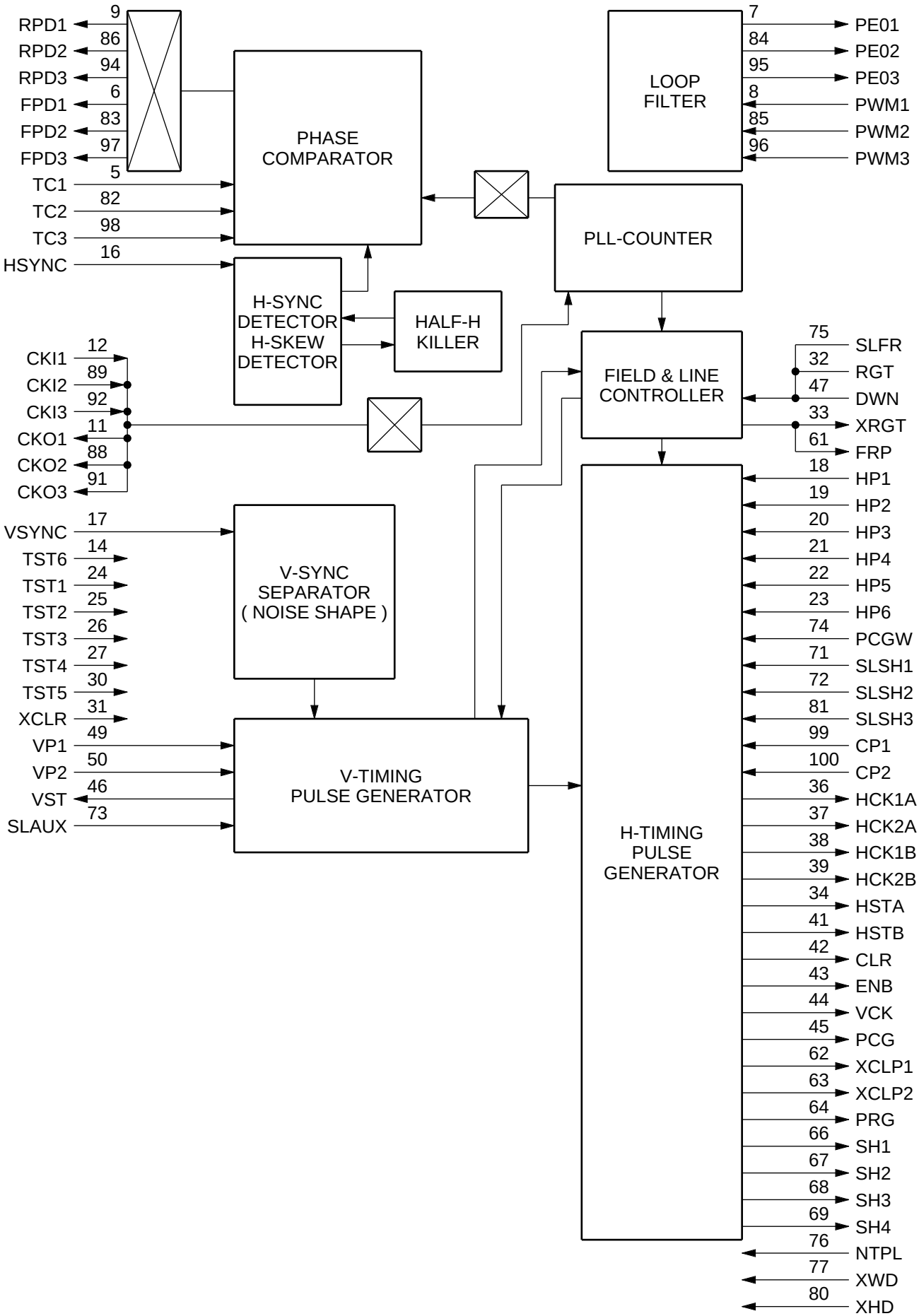


INPUT

CKI1	; OSCILLATION CELL FOR NTSC/PAL
CKI2	; OSCILLATION CELL FOR WIDE
CKI3	; OSCILLATION CELL FOR HD/MNDC
CP1,CP2	; PEDESTAL CLAMP POSITION SELECT
DWN	; IDENTIFYING SIGNAL TO TURN UPSIDE DOWN
HP1-HP6	; HORIZONTAL DISPLAY START POSITION SELECT
HSYNC	; H SYNC (NEGATIVE POLARITY)
NTPL	; MODE SELECT
PCGW	; PCG SELECT
PWM1	; INTEGRATOR INPUT 1 FOR LOOP FILTER
PWM2	; INTEGRATOR INPUT 2 FOR LOOP FILTER
PWM3	; INTEGRATOR INPUT 3 FOR LOOP FILTER
RGT	; IDENTIFYING SIGNAL TO TURN THE LEFT AND RIGHT SIDE
SLAUX	; FREE RUN IDENTIFYING LINE NUMBER SELECT
SLFR	; H REVERSE / F REVERSE SELECT (H: H REVERSE, L: F REVERSE)
SLSH1-SLSH3	; SAMPLE HOLD SELECT
TC1	; PULSE WIDTH ADJUSTMENT FOR FPD1 TERMINAL
TC2	; PULSE WIDTH ADJUSTMENT FOR FPD2 TERMINAL
TC3	; PULSE WIDTH ADJUSTMENT FOR FPD3 TERMINAL
TST1-TST6	; TEST
VP1,VP2	; VERTICAL DISPLAY START POSITION SELECT
VSYNC	; V SYNC (NEGATIVE POLARITY)
XCLR	; CLEAR (AT 0V)
XHD	; MODE SELECT
XWD	; MODE SELECT

OUTPUT

CKO1	; OSCILLATION CELL FOR NTSC/PAL
CKO2	; OSCILLATION CELL FOR WIDE
CKO3	; OSCILLATION CELL FOR HD/MNDC
CLR	; CLEAR PULSE
ENB	; ENABE PULSE
FPD1	; PHASE COMPARATOR OUTPUT B-1 FOR NTSC/PAL
FPD2	; PHASE COMPARATOR OUTPUT B-2 FOR WIDE
FPD3	; PHASE COMPARATOR OUTPUT B-3 FOR HD/MNDC
FRP	; ALTERNATING CURRENT DRIVE REVERSE TIMING
HCK1A	; H CLOCK PULSE 1A
HCK1B	; H CLOCK PULSE 1B
HCK2A	; H CLOCK PULSE 2A
HCK2B	; H CLOCK PULSE 2B
HSTA	; H START PULSE A
HSTB	; H START PULSE B
PCG	; PRECHAGE PULSE
PEO1	; INTEGRATOR OUTPUT 1 FOR LOOP FILTER
PEO2	; INTEGRATOR OUTPUT 2 FOR LOOP FILTER
PEO3	; INTEGRATOR OUTPUT 3 FOR LOOP FILTER
PRG	; PRECHAGE SIGNAL PULSE
RPD1	; PHASE COMPARATOR OUTPUT A-1 FOR NTSC/PAL
RPD2	; PHASE COMPARATOR OUTPUT A-2 FOR WIDE
RPD3	; PHASE COMPARATOR OUTPUT A-3 FOR HD/MNDC
SH1	; SAMPLE HOLD PULSE 1
SH2	; SAMPLE HOLD PULSE 2
SH3	; SAMPLE HOLD PULSE 3
SH4	; RESAMPLE HOLD PULSE
VCK	; V CLOCK PULSE
VST	; V START PULSE
XCLP1	; PEDESTAL CLAMP PULSE 1 FOR VIDEO SIGNAL
XCLP2	; PEDESTAL CLAMP PULSE 2 FOR VIDEO SIGNAL
XRGT	; IDENTIFYING SIGNAL TO TURN THE LEFT AND RIGHT SIDE


RPD1
RPD2
RPD3
FPD1
FPD2
FPD3
TC1
TC2
TC3
HSYNC
9
86
94
6
83
97
5
82
98
16
PHASE COMPARATOR
LOOP FILTER
7
84
95
8
85
96
PE01
PE02
PE03
PWM1
PWM2
PWM3
PLL-COUNTER
H-SYNC DETECTOR H-SKEW DETECTOR
HALF-H KILLER
CKI1
CKI2
CKI3
CKO1
CKO2
CKO3
12
89
92
11
88
91
FIELD & LINE CONTROLLER
75
32
47
33
61
SLFR
RGT
DWN
XRGT
FRP
VSYNC
TST6
TST1
TST2
TST3
TST4
TST5
XCLR
VP1
VP2
VST
SLAUX
17
14
24
25
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27
30
31
49
50
46
73
V-SYNC SEPARATOR (NOISE SHAPE)
V-TIMING PULSE GENERATOR
H-TIMING PULSE GENERATOR
18
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21
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74
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72
81
99
100
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37
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44
45
62
63
64
66
67
68
69
76
77
80
HP1
HP2
HP3
HP4
HP5
HP6
PCGW
SLSH1
SLSH2
SLSH3
CP1
CP2
HCK1A
HCK2A
HCK1B
HCK2B
HSTA
HSTB
CLR
ENB
VCK
PCG
XCLP1
XCLP2
PRG
SH1
SH2
SH3
SH4
NTPL
XWD
XHD