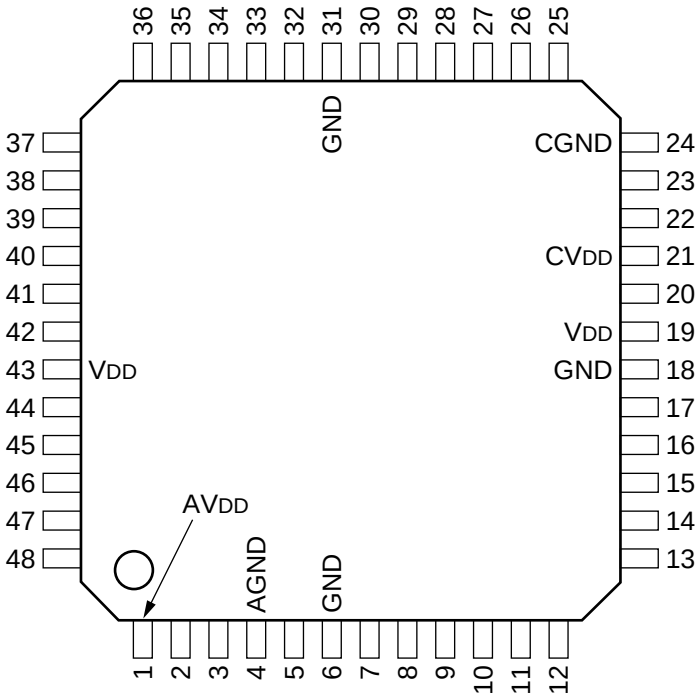
C-MOS TIMING CONTROLLER FOR CCD CAMERAS

—TOP VIEW—



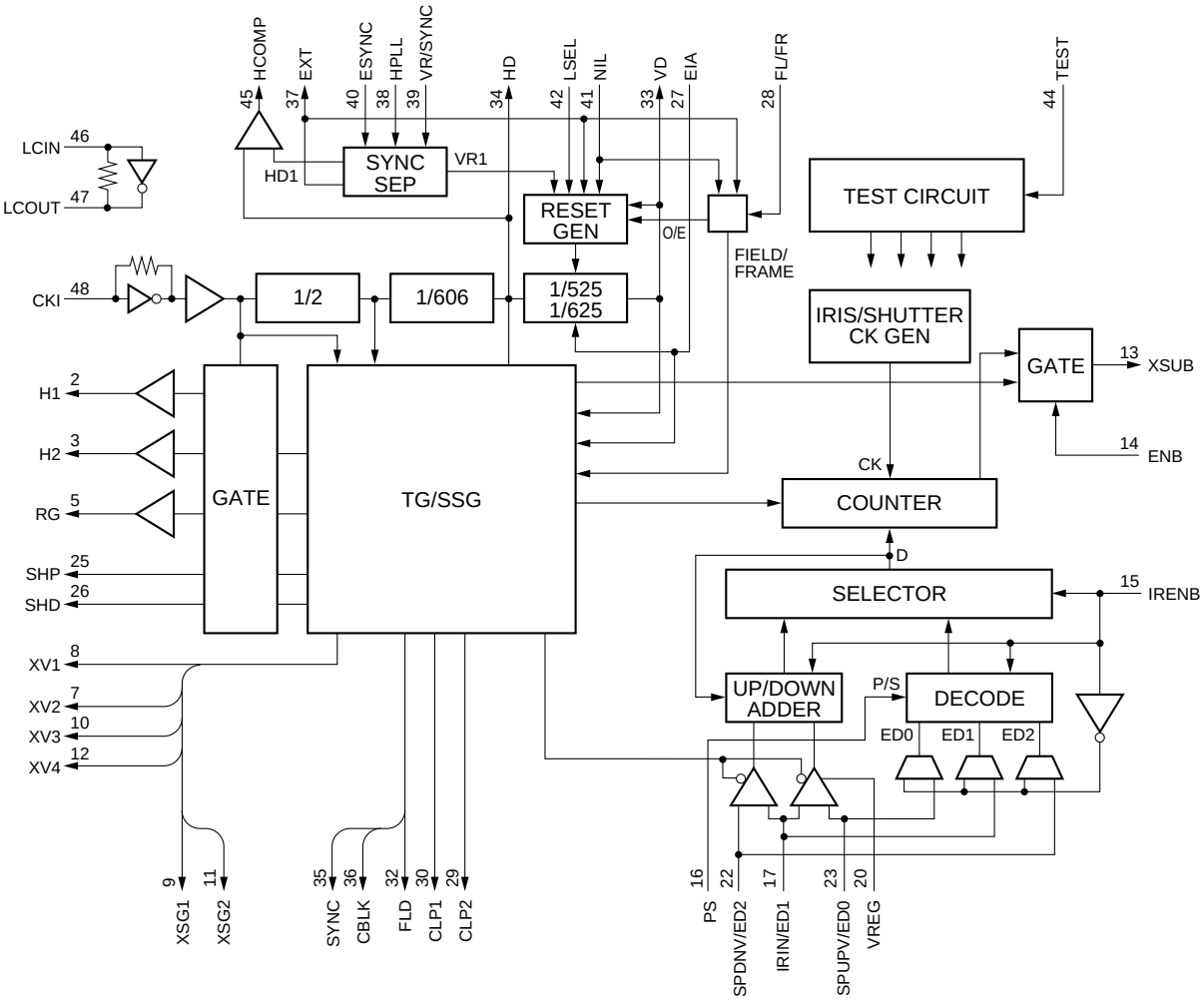
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	AV_{DD}	13	O	XSUB	25	O	SHP	37	O	EXT
2	O	H1	14	I	ENB	26	O	SHD	38	I	HPLL
3	O	H2	15	I	IRENB	27	I	EIA	39	I	VR/SYNC
4	—	AGND	16	I	PS	28	I	FL/FR	40	I	ESYNC
5	O	RG	17	I	IRIN/ED1	29	O	CLP2	41	I	NIL
6	—	GND	18	—	GND	30	O	CLP1	42	I	LSEL
7	O	XV2	19	—	V_{DD}	31	—	GND	43	—	V_{DD}
8	O	XV1	20	—	VREG	32	O	FLD	44	I	TEST
9	O	XSG1	21	I	CV_{DD}	33	O	VD	45	O	HCOMP
10	O	XV3	22	I	SPDNV/ED2	34	O	HD	46	I	LCIN
11	O	XSG2	23	I	SPUPV/ED0	35	O	SYNC	47	O	LCOUT
12	O	XV4	24	—	CGND	36	O	CBLK	48	I	CKI

INPUT

CKI	:	CLOCK
ED0 - ED2	:	SHUTTER SPEED SETTING
EIA	:	EIA/CCIR SYSTEM SELECT
ENB	:	ON/OFF CONTROL OF XSUB SIGNAL
ESYNC	:	SYNC LOCK SELECT SIGNAL
FL/FR	:	ODD/EVEN FIELD SELECT
HPLL	:	HORIZONTAL DRIVE SIGNAL
IRENB	:	ELECTRONIC SHUTTER/IRIS MODE SELECT
IRIN	:	IRIS SIGNAL
LCIN	:	INVERTING INPUT FOR OSCILLATOR
LSEL	:	LINE SELECT
NIL	:	INTERLACE MODE SELECT
PS	:	ELECTRONIC SHUTTER SPEED INPUT METHOD SELECT
SPDNV	:	REFERENCE VOLTAGE FOR DECREASING THE SHUTTER SPEED
SPUPV	:	REFERENCE VOLTAGE FOR INCREASING THE SHUTTER SPEED
TEST	:	TEST
VR/SYNC	:	VERTICAL DRIVE/COMPOSITE SYNC SIGNAL
VREG	:	COMPARATOR'S BIAS CURRENT

OUTPUT

CBLK	:	COMPOSITE BLANKING SIGNAL
CLP1, CLP2	:	CLAMP PULSE
EXT	:	EXT SYNC/INT SYNC DISCRIMINATION SIGNAL
FLD	:	ODD/EVEN FIELD DISCRIMINATION SIGNAL
H1, H2	:	CCD'S HORIZONTAL REGISTER DRIVING CLOCK
HCOMP	:	HORIZONTAL COMPARATOR
HD	:	HORIZONTAL DRIVE SIGNAL
LCOUT	:	INVERTING OUTPUT FOR OSCILLATOR
RG	:	RESET GATE PULSE
SHD	:	SAMPLE AND HOLD PULSE FOR DATA
SHP	:	SAMPLE AND HOLD PULSE PRE-CHARGE LEVEL
SYNC	:	COMPOSITE SYNC SIGNAL
VD	:	VERTICAL DRIVE SIGNAL
XSG1, XSG2	:	CCD SENSOR'S ELECTRON CHARGE READ OUT PULSE
XSUB	:	CCD'S ELECTRON CHARGE WIPE OUT PULSE
XV1 - XV4	:	CCD'S VERTICAL REGISTER DRIVING CLOCK


HCOMP
EXT
ESYNC
HPLL
VR/SYNC
HD
LSEL
NIL
VD
EIA
FL/FR
TEST
45
37
40
38
39
34
42
41
33
27
28
44
LCIN
46
LCOUT
47
HD1
SYNC SEP
VR1
RESET GEN
O/E
FIELD/ FRAME
TEST CIRCUIT
CKI
48
1/2
1/606
1/525 1/625
IRIS/SHUTTER CK GEN
GATE
13
XSUB
14
ENB
H1
2
H2
3
RG
5
SHP
25
SHD
26
GATE
TG/SSG
CK
COUNTER
D
SELECTOR
15
IRENB
XV1
8
XV2
7
XV3
10
XV4
12
UP/DOWN ADDER
P/S
DECODE
ED0
ED1
ED2
9
11
35
36
32
30
29
16
22
17
23
20
XSG1
XSG2
SYNC
CBLK
FLD
CLP1
CLP2
PS
SPDNV/ED2
IRIN/ED1
SPUPV/ED0
VREG