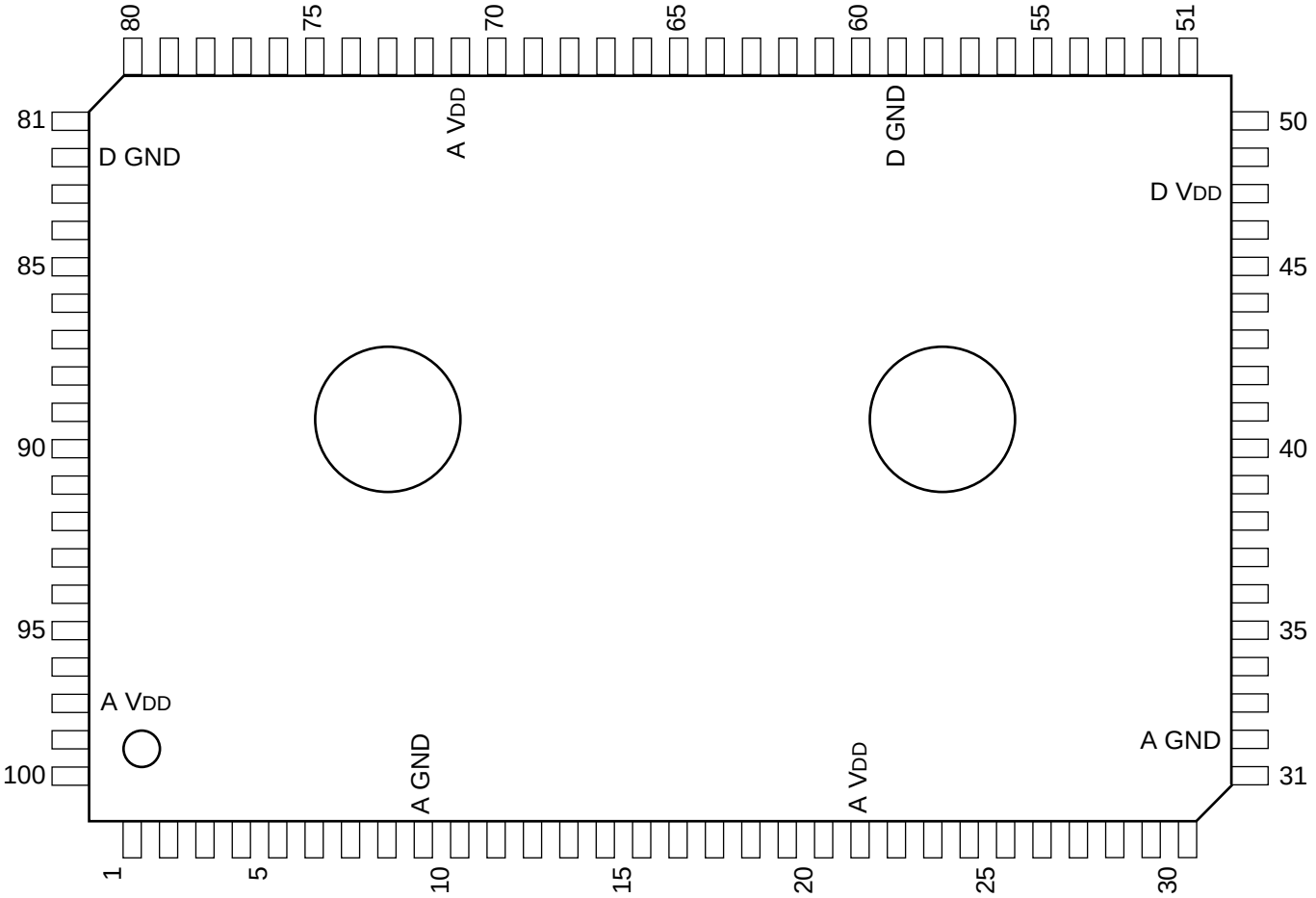
C-MOS WRITE CLOCK GENERATORE FOR TBC

—TOP VIEW—



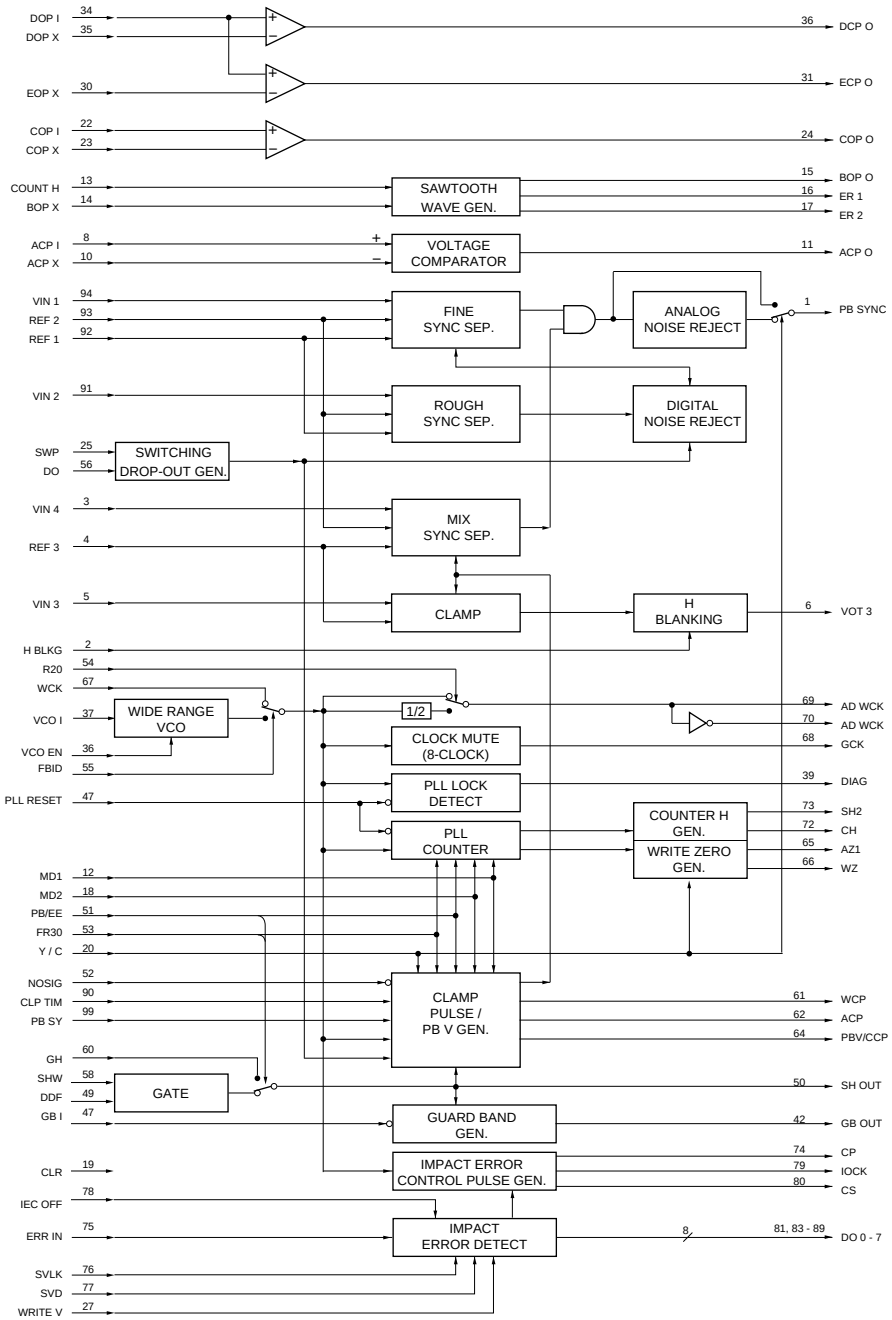
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	PB SYNC	21	—	A VDD	41	O	ADSW	61	O	WCP	81	O	DO 0
2	I	H BLKG	22	I	COP I	42	O	GB OUT	62	O	ACP	82	—	D GND
3	I	VIN 4	23	I	COP X	43	O	TEST OUT0	63	O	TOUT	83	O	DO 1
4	I	REF 3	24	O	COP O	44	O	TEST OUT1	64	O	PBV/CCP	84	O	DO 2
5	I	VIN 3	25	I	SWP	45	I	TEST IN2	65	O	AZ1	85	O	DO 3
6	O	VOT 3	26	I	TST	46	I	TEST IN3	66	O	WZ	86	O	DO 4
7	I	AI 3	27	I	WRITE V	47	I	$\overline{\text{PLL RESET}}$	67	I	WCK	87	O	DO 5
8	I	ACPI	28	I	$\overline{\text{TEST0}}$	48	—	D VDD	68	O	GCK	88	O	DO 6
9	—	A GND	29	I	TEST1	49	I	DDF	69	O	AD WCK	89	O	DO 7
10	I	ACP X	30	I	EOP X	50	O	SH OUT	70	O	$\overline{\text{AD WCK}}$	90	I	CLP TIM
11	O	ACP O	31	O	EOP O	51	I	$\overline{\text{PB}}$/EE	71	—	D VDD	91	I	VIN 2
12	I	MD1	32	—	A GND	52	I	$\overline{\text{NOSIG}}$	72	O	CH	92	I	REF 1
13	I	COUNT H	33	I	AI 2	53	I	$\overline{\text{FR30}}$	73	O	SH2	93	I	REF 2
14	I	BOP X	34	I	DOP I	54	I	$\overline{\text{R20}}$	74	O	CP	94	I	VIN 1
15	O	BOP O	35	I	DOP X	55	I	$\overline{\text{FBID}}$	75	I	ERR IN	95	I	AOP I
16	O	ER 1	36	O	DOP O	56	I	DO	76	I	SVLK	96	I	AOP X
17	O	ER 2	37	I	VCO I	57	I	GBI	77	I	SVD	97	O	AOP O
18	I	MD2	38	I	VCO EN	58	I	SHW	78	I	IEC OFF	98	—	A VDD
19	I	CLR	39	O	DIAG	59	—	D GND	79	O	IOCK	99	I	PB SY
20	I	Y/$\overline{\text{C}}$	40	I	DSEL	60	I	GH	80	O	CS	100	I	CCP I

INPUT

ACP I	;	COMPARATOR (+)
ACP X	;	COMPARATOR (–)
AI 2, 3	;	CURRENT SOURCE
AOP I	;	OP AMP A (+) (REFERENCE VOLTAGE 0.7 V)
AOP X	;	OP AMP A (–) FOR SAWTOOTH WAVE GENERATION OF PB SYNC NOISE REJECTOR
BOP X	;	OP AMP B (–) FOR SAWTOOTH WAVE GENERATION OF PLL PHASE COMPARATOR
CCPI	;	REFERENCE VOLTAGE (3.8 V)
CLP TIM	;	CHROMA WRITE CLAMP PULSE TIMING SHIFT
CLR	;	CLEAR
COP I	;	OP AMP C (+)
COP X	;	OP AMP C (–)
COUNT H	;	COUNT H
DDF	;	DOUBLE-DIFFERENTIAL PULSE
DO	;	DROP-OUT PULSE
DOP I	;	REFERENCE VOLTAGE INPUT FOR PLL ERROR AMP
DOP X	;	PLL ERROR AMP INPUT 2
DSEL	;	A/D SELECT (CONNECT TO PIN 41)
EOP X	;	PLL ERROR AMP INPUT 1
ERR IN	;	ERROR IN (8 BITS, SERIAL) FROM IMPACT ERROR COMPENSATION
$\overline{\text{FBID}}$	;	FAST BIDIREX MODE
$\overline{\text{FR30}}$	;	FORWARD/REVERSE 30 OR OVER TIMES MODE
$\overline{\text{GBI}}$	;	GUARD BAND (H ; PLL PHASE COMPARATE ENABLE)
GH	;	GATED H
H BLKG	;	H BLANKING PULSE
IEC OFF	;	IMPACT ERROR COMPENSATION DISABLE
MD1	;	MODE SELECT (H ; 525, L ; 625)
MD2	;	MODE SELECT (H ; 13.5 MHz, L ; 14.3 MHz)
$\overline{\text{NOSIG}}$	;	NO SIGNAL STATUS
$\overline{\text{PB}}$ SY	;	PB SYNC
PB/EE	;	MODE SELECT (H ; E-E MODE, L ; PB MODE)
$\overline{\text{PLL RESET}}$	;	PLL COUNTER RESET
$\overline{\text{R20}}$	;	FREQUENCY CONTROL OF AD WCK (L ; HALF, H ; NORMAL)
REF 1	;	CLAMP LEVEL IN FOR SYNC SEPARATOR
REF 2	;	SLICE LEVEL IN FOR SYNC SEPARATOR
REF 3	;	CLAMP LEVEL IN FOR H BLANKING GENERATOR
SHW	;	SWITCHING WINDOW PULSE
SVD	;	SERVO LOCK VD
SVLK	;	SERVO LOCK SIGNAL
SWP	;	SWITCHING PULSE
TEST IN 2, 3	;	FOR TEST
TEST0, 1	;	FOR TEST
TST	;	FOR TEST
VCO EN	;	INTERNAL VCO ENABLE
VCO I	;	INTERNAL VCO ERROR VOLTAGE
VIN 1	;	VIDEO IN FOR FINE SYNC SEPARATOR
VIN 2	;	VIDEO IN FOR ROUGH SYNC SEPARATOR
VIN 3	;	VIDEO IN FOR H BLANKING GENERATOR
VIN 4	;	VIDEO IN FOR MIX SYNC SEPARATOR
WCK	;	WRITE CLOCK
WRITE V	;	WRITE V
Y/$\overline{\text{C}}$	;	MODE SELECT (H ; Y MODE, L ; C MODE)

OUTPUT

ACP	;	ADVACE WRITE CLAMP PULSE
ACP O	;	COMPARATOR
AD WCK	;	WRITE CLOCK FOR A/D CONVERTER
ADSW	;	A/D SWITCH (CONNECT TO PIN 40)
AOP O	;	A SAWTOOTH WAVE FOR PB SYNC NOISE REJECT
AZ1	;	ADVANCE WRITE ZERO
BOP O	;	A SAWTOOTH WAVE FOR PLL PHASE COMPARATE
CH	;	COUNT H
CP	;	CLAMP PULSE FOR IMPACT ERROR COMPENSATION
CS	;	CHIP SELECT FOR IMPACT ERROR A/D CONVERTR
DIAG	;	DIAGNOSTIC
DO 0 - 7	;	IMPACT ERROR COMPENSATION DATA (8 BITS)
DOP O	;	PLL ERROR AMP OUTPUT 2
ER 1	;	PLL ERROR
ER 2	;	AFC ERROR
EOP O	;	PLL ERROR AMP OUTPUT 1
GB OUT	;	GUARD BAND
GCK	;	GATED WRITE CLOCK
IOCK	;	CLOCK FOR IMPACT ERROR A/D CONVERTER
PB SYNC	;	PB SYNC
PBV/CCP	;	Y MODE; PB V
		C MODE; CENTER WRITE CLAMP PULSE FOR CTDM SIGNAL
SH OUT	;	SAMPLING & HOLD PULSE
SH2	;	SAMPLING PULSE FOR AFC
TEST OUT0, 1	;	FOR TEST
TOUT	;	FOR TEST
VOT 3	;	H BLANKING
WCP	;	WRITE CLAMP PULSE
WZ	;	WRITE ZERO


DOP I
DOP X
EOP X
COP I
COP X
COUNT H
BOP X
ACP I
ACP X
VIN 1
REF 2
REF 1
VIN 2
SWP
DO
VIN 4
REF 3
VIN 3
H BLKG
R20
WCK
VCO I
VCO EN
FBID
PLL RESET
MD1
MD2
PB/EE
FR30
Y / C
NOSIG
CLP TIM
PB SY
GH
SHW
DDF
GB I
CLR
IEC OFF
ERR IN
SVLK
SVD
WRITE V
DCP O
ECP O
COP O
BOP O
ER 1
ER 2
ACP O
PB SYNC
VOT 3
AD WCK
AD WCK
GCK
DIAG
SH2
CH
AZ1
WZ
WCP
ACP
PBV/CCP
SH OUT
GB OUT
CP
IOCK
CS
DO 0 - 7
SAWTOOTH WAVE GEN.
VOLTAGE COMPARATOR
FINE SYNC SEP.
ROUGH SYNC SEP.
MIX SYNC SEP.
CLAMP
SWITCHING DROP-OUT GEN.
WIDE RANGE VCO
1/2
CLOCK MUTE (8-CLOCK)
PLL LOCK DETECT
PLL COUNTER
GATE
GUARD BAND GEN.
IMPACT ERROR CONTROL PULSE GEN.
IMPACT ERROR DETECT
CLAMP PULSE / PB V GEN.
ANALOG NOISE REJECT
DIGITAL NOISE REJECT
H BLANKING
COUNTER H GEN.
WRITE ZERO GEN.