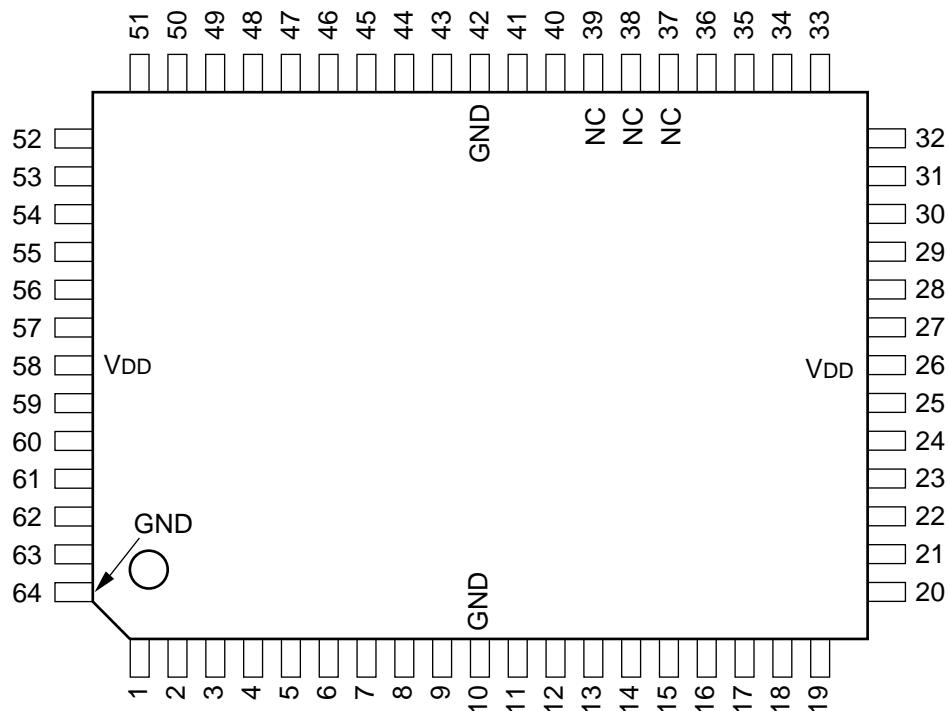


C-MOS DROP-OUT COMPENSATOR

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	DTIN0	17	I	PB O/Ē	33	I	TEST1	49	O	DOTB1
2	I	DTIN1	18	I	V TIMING	34	I	TEST2	50	O	DOTB0
3	I	DTIN2	19	I	THRU	35	I	TEST3	51	—	GND
4	I	DTIN3	20	I	SECAM	36	I	SHIFT	52	O	DOTA9
5	I	DTIN4	21	I	DT	37	—	NC	53	O	DOTA8
6	I	DTIN5	22	I	BID	38	—	NC	54	O	DOTA7
7	I	DTIN6	23	I	ADDINH	39	—	NC	55	O	DOTA6
8	I	DTIN7	24	I	DOCINH	40	O	DOTB9	56	O	DOTA5
9	I	DTIN8	25	I	2LDOC	41	O	DOTB8	57	O	DOTA4
10	—	GND	26	—	VDD	42	—	GND	58	—	VDD
11	I	DTIN9	27	I	U/D	43	O	DOTB7	59	O	DOTA3
12	I	RCK	28	I	MOD1	44	O	DOTB6	60	O	DOTA2
13	I	B-Y	29	I	MOD2	45	O	DOTB5	61	O	DOTA1
14	I	HSYNC	30	I	MOD3	46	O	DOTB4	62	O	DOTA0
15	I	ADVVBBLK	31	I	MOD4	47	O	DOTB3	63	I	OE
16	I	REF O/Ē	32	I	CLR	48	O	DOTB2	64	—	GND

11	DTIN9	DOTA9	52	INPUT	
9	DTIN8	DOTA8	53	2LDOC	; 2 LINE DOC
8	DTIN7	DOTA7	54	ADDINH	; ADD INHIBIT
7	DTIN6	DOTA6	55	ADVBLK	; ADVANCED V-BLANKING
6	DTIN5	DOTA5	56	B-Y	; B- \bar{Y} /R-Y
5	DTIN4	DOTA4	57	BID	; VARIABLE PLAY MODE
4	DTIN3	DOTA3	59	CLR	; CLEAR
3	DTIN2	DOTA2	60	DOCINH	; DROP-OUT COMPENSATION INHIBIT
2	DTIN1	DOTA1	61	DT	; DT MODE
1	DTIN0	DOTA0	62	DTIN9 - DTIN0	; 10-BIT VIDEO DATA INPUTS
12	RCK			HSYNC	; H TIMING PULSE
13	B-Y	DOTB9	40	MOD1 - MOD4	; MODE CONTROL
14	Hsync	DOTB8	41	OE	; OUTPUT ENABLE
15	ADVBLK	DOTB7	43	PB O/ \bar{E}	; PB ODD/EVEN
16	REF O/ \bar{E}	DOTB6	44	RCK	; SYSTEM CLOCK
17	PB O/ \bar{E}	DOTB5	45	REF O/ \bar{E}	; SECAM MODE
18	V TIMING	DOTB4	46	SECAM	; SHIFT MODE
19	THRU	DOTB3	47	SHIFT	; TEST CONTROL
20	SECAM	DOTB2	48	TEST1 - TEST3	; DATA THROUGH
21	DT	DOTB1	49	THRU	; 1H UP/DOWN
22	BID	DOTB0	50	U/D	; V TIMING PULSE
23	ADDINH			V TIMING	
24	DOCINH				
25	2LDOC				
27	U/D				
28	MOD1				
29	MOD2				
30	MOD3				
31	MOD4				
32	CLR				
36	SHIFT				
33	TEST1				
34	TEST2				
35	TEST3				
63	OE				