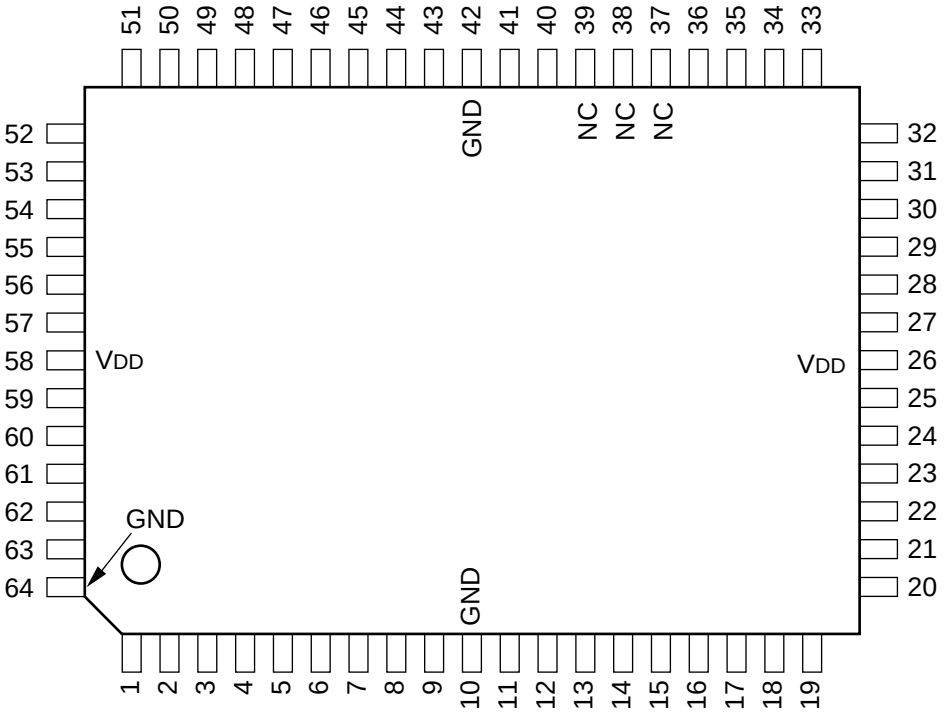
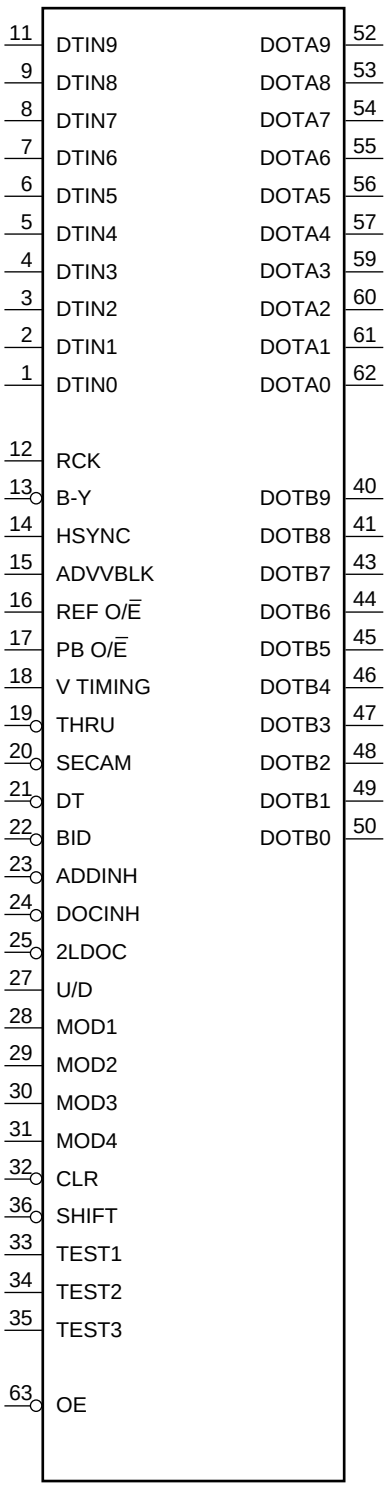
C-MOS DROP-OUT COMPENSATOR

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	DTIN0	17	I	PB O/$\overline{E}$	33	I	TEST1	49	O	DOTB1
2	I	DTIN1	18	I	V TIMING	34	I	TEST2	50	O	DOTB0
3	I	DTIN2	19	I	$\overline{THRU}$	35	I	TEST3	51	—	GND
4	I	DTIN3	20	I	$\overline{SECAM}$	36	I	$\overline{SHIFT}$	52	O	DOTA9
5	I	DTIN4	21	I	$\overline{DT}$	37	—	NC	53	O	DOTA8
6	I	DTIN5	22	I	$\overline{BID}$	38	—	NC	54	O	DOTA7
7	I	DTIN6	23	I	$\overline{ADDINH}$	39	—	NC	55	O	DOTA6
8	I	DTIN7	24	I	$\overline{DOCINH}$	40	O	DOTB9	56	O	DOTA5
9	I	DTIN8	25	I	$\overline{2LDOC}$	41	O	DOTB8	57	O	DOTA4
10	—	GND	26	—	V_{DD}	42	—	GND	58	—	V_{DD}
11	I	DTIN9	27	I	U/D	43	O	DOTB7	59	O	DOTA3
12	I	RCK	28	I	MOD1	44	O	DOTB6	60	O	DOTA2
13	I	$\overline{B\text{-}Y}$	29	I	MOD2	45	O	DOTB5	61	O	DOTA1
14	I	HSYNC	30	I	MOD3	46	O	DOTB4	62	O	DOTA0
15	I	ADVVBLK	31	I	MOD4	47	O	DOTB3	63	I	$\overline{OE}$
16	I	REF O/$\overline{E}$	32	I	$\overline{CLR}$	48	O	DOTB2	64	—	GND



INPUT

2LDOC	;	2 LINE DOC
ADDINH	;	ADD INHIBIT
ADVVBLK	;	ADVANCED V-BLANKING
B-Y	;	$\overline{\text{B-Y}}$/R-Y
BID	;	VARIABLE PLAY MODE
CLR	;	CLEAR
DOCINH	;	DROP-OUT COMPENSATION INHIBIT
DT	;	DT MODE
DTIN9 - DTIN0	;	10-BIT VIDEO DATA INPUTS
HSYNC	;	H TIMING PULSE
MOD1 - MOD4	;	MODE CONTROL
OE	;	OUTPUT ENABLE
PB O/$\overline{\text{E}}$	;	PB ODD/EVEN
RCK	;	SYSTEM CLOCK
REF O/$\overline{\text{E}}$	;	SECAM MODE
SECAM	;	SHIFT MODE
SHIFT	;	TEST CONTROL
TEST1 - TEST3	;	DATA THROUGH
THRU	;	1H UP/DOWN
U/D	;	V TIMING PULSE
V TIMING		

OUTPUT

DOTA9 - DOTA0	;	10-BIT VIDEO DATA OUTPUTS-A
DOTB9 - DOTB0	;	10-BIT VIDEO DATA OUTPUTS-B