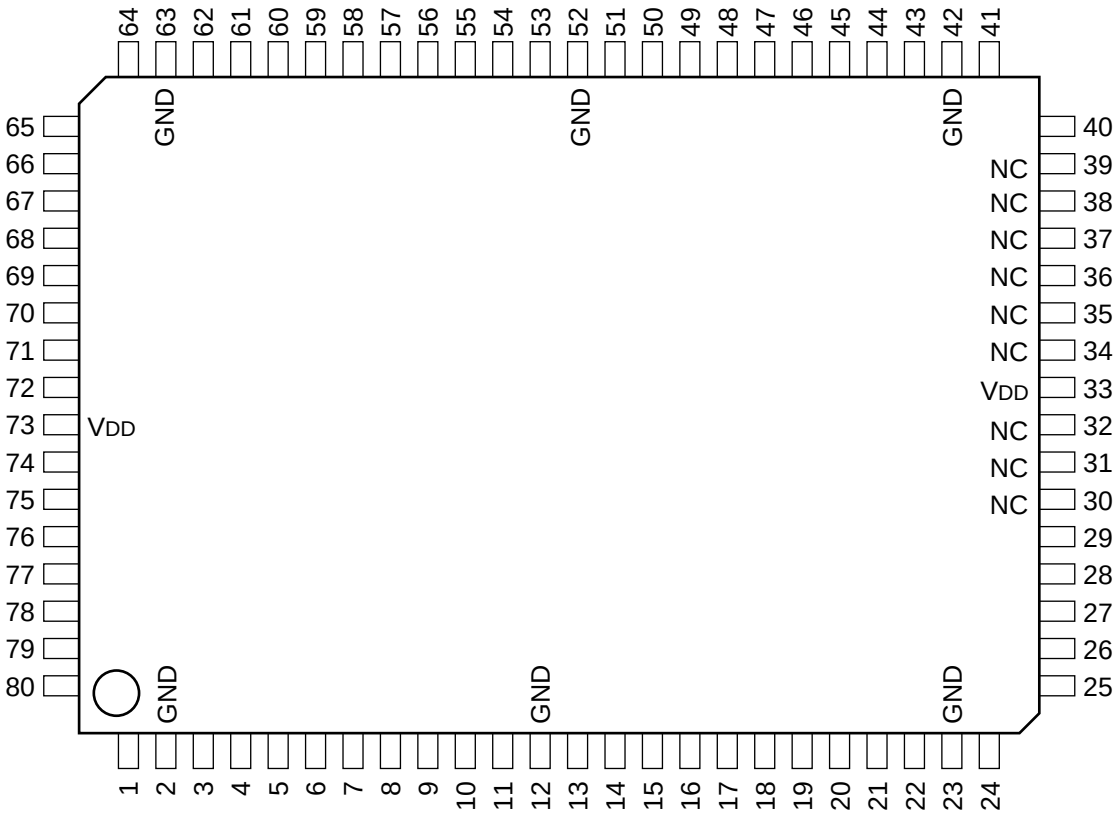
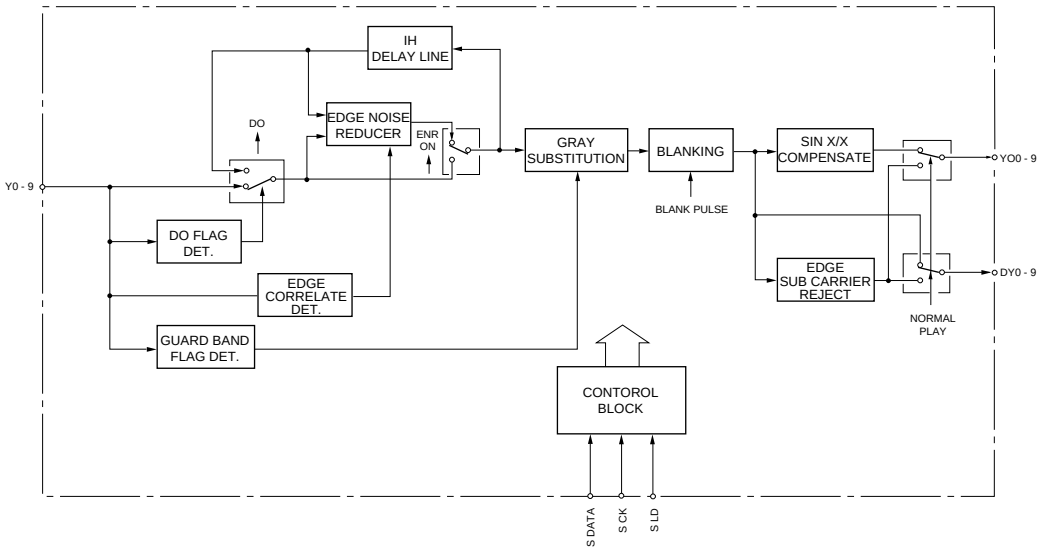
C-MOS DIGITAL EDGE NOISE REDUCER

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	Y0	21	I	$\overline{DT}$	41	O	YO0	61	O	DY8
2	—	GND	22	I	D0	42	—	GND	62	O	DY9
3	I	CK	23	—	GND	43	O	YO1	63	—	GND
4	I	$\overline{BID}$	24	I	D1	44	O	YO2	64	I	$\overline{OE2}$
5	I	$\overline{CBLK}$	25	I	ENS1	45	O	YO3	65	I	DTSTB
6	I	$\overline{VBLK}$	26	I	DNS0	46	O	YO4	66	I	SLD
7	I	H SYN	27	I	MOD1	47	O	YO5	67	I	SDATA
8	I	$\overline{VISC\ EX}$	28	I	MOD2	48	O	YO6	68	I	SCK
9	I	$\overline{X30}$	29	I	MODS	49	O	YO7	69	O	STP
10	I	$\overline{SW1}$	30	—	NC	50	O	YO8	70	O	S OUT
11	I	$\overline{GRSW}$	31	—	NC	51	O	YO9	71	I	Y9
12	—	GND	32	—	NC	52	—	GND	72	I	Y8
13	I	$\overline{ENROFF}$	33	—	VDD	53	O	DY0	73	—	VDD
14	I	$\overline{ESROFF}$	34	—	NC	54	O	DY1	74	I	Y7
15	I	$\overline{DEF}$	35	—	NC	55	O	DY2	75	I	Y6
16	I	MUTE1	36	—	NC	56	O	DY3	76	I	Y5
17	I	MUTE3	37	—	NC	57	O	DY4	77	I	Y4
18	I	$\overline{DIG\ IF}$	38	—	NC	58	O	DY5	78	I	Y3
19	I	$\overline{3S4}$	39	—	NC	59	O	DY6	79	I	Y2
20	I	$\overline{APOFF}$	40	I	$\overline{OE1}$	60	O	DY7	80	I	Y1


IH
DELAY LINE
EDGE NOISE
REDUCER
DO
ENR
ON
GRAY
SUBSTITUTION
BLANKING
SIN X/X
COMPENSATE
YO0 - 9
Y0 - 9
BLANK PULSE
DO FLAG
DET.
EDGE
SUB CARRIER
REJECT
DY0 - 9
EDGE
CORRELATE
DET.
NORMAL
PLAY
GUARD BAND
FLAG DET.
CONTOROL
BLOCK
S DATA
S CK
S LD