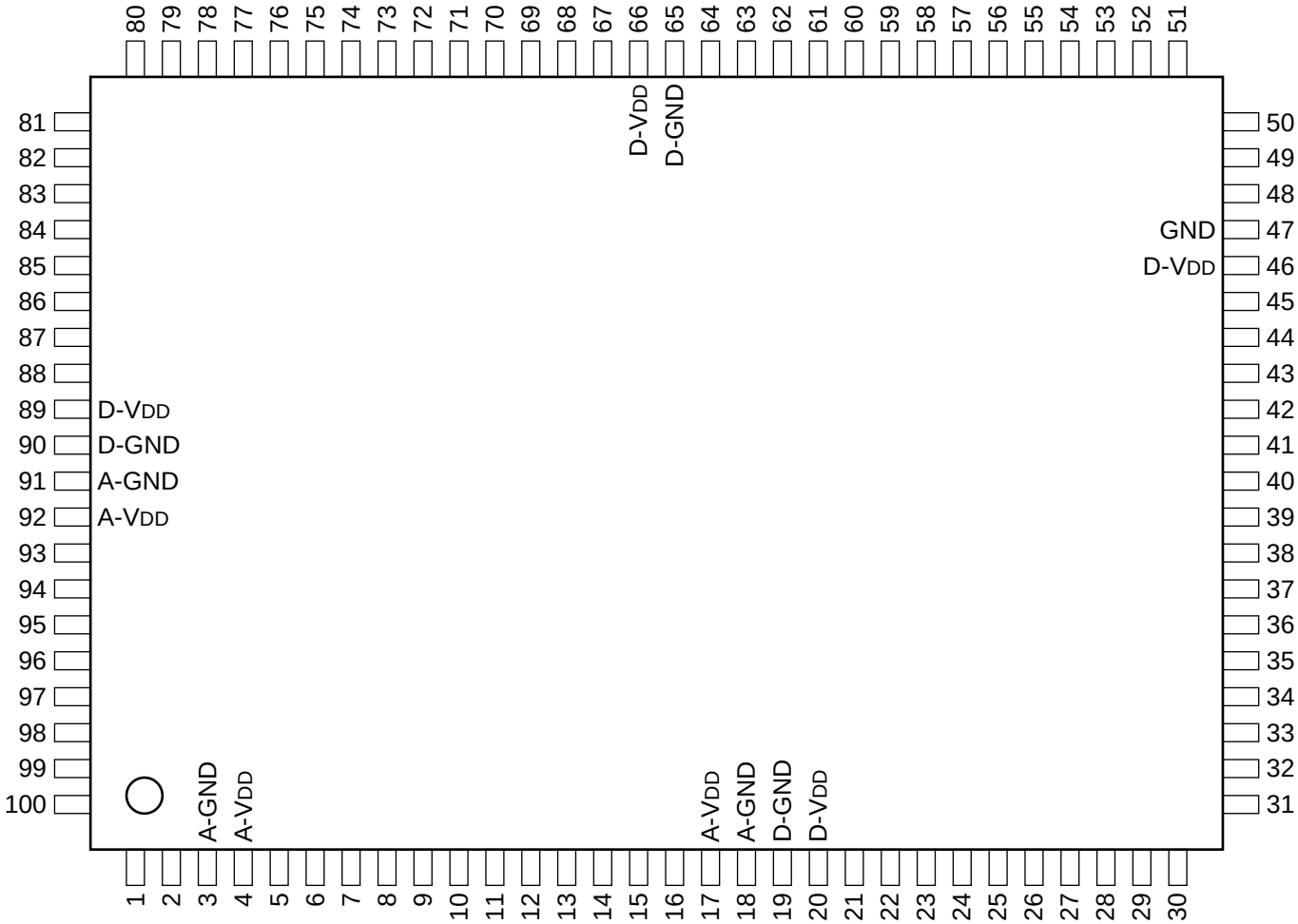
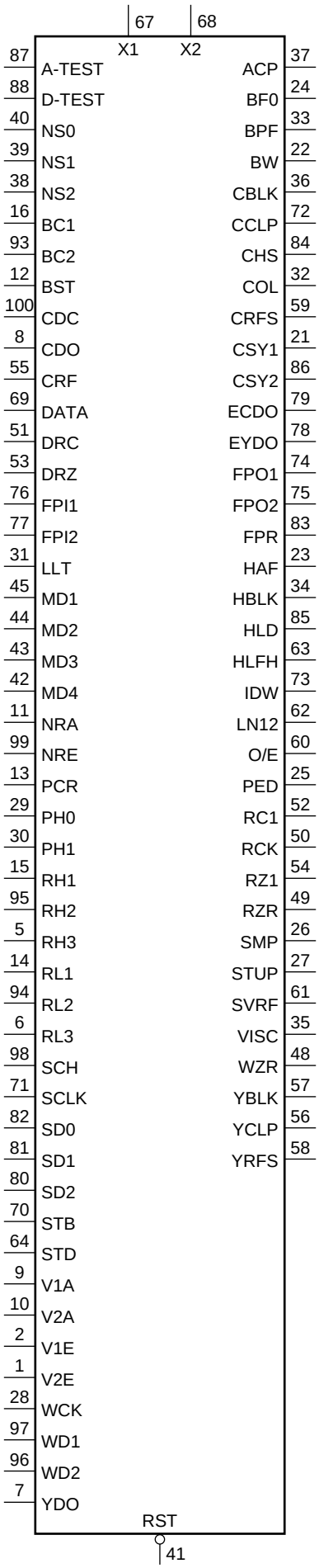
C-MOS Y/C SEPARATOR/CLOCK GENERATOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	V2E	26	O	SMP	51	I	DRC	76	I	FPI1
2	I	V1E	27	O	STUP	52	O	RC1	77	I	FPI2
3	—	A-GND	28	I	WCK	53	I	DRZ	78	O	EYDO
4	—	A-V_{DD}	29	I	PH0	54	O	RZ1	79	O	ECDO
5	I	RH3	30	I	PH1	55	I	CRF	80	I	SD2
6	I	RL3	31	I	LLT	56	O	YCLP	81	I	SD1
7	I	YDO	32	O	COL	57	O	YBLK	82	I	SD0
8	I	CDO	33	O	BPF	58	O	YRFS	83	O	FPR
9	I	V1A	34	O	HBLK	59	O	CRFS	84	O	CHS
10	I	V2A	35	O	VISC	60	O	O/E	85	O	HLD
11	I	NRA	36	O	CBLK	61	O	SVRF	86	O	CSY2
12	I	BST	37	O	ACP	62	O	LN12	87	I	A-TEST
13	I	PCR	38	I	NS2	63	O	HLFH	88	I	D-TEST
14	I	RL1	39	I	NS1	64	I	STD	89	—	D-V_{DD}
15	I	RH1	40	I	NS0	65	—	D-GND	90	—	D-GND
16	I	BC1	41	I	$\overline{\text{RST}}$	66	—	D-V_{DD}	91	—	A-GND
17	—	A-V_{DD}	42	I	MD4	67	I	X1	92	—	A-V_{DD}
18	—	A-GND	43	I	MD3	68	O	X2	93	I	BC2
19	—	D-GND	44	I	MD2	69	I	DATA	94	I	RL2
20	—	D-V_{DD}	45	I	MD1	70	I	STB	95	I	RH2
21	O	CSY1	46	—	D-V_{DD}	71	I	SCLK	96	I	WD2
22	O	BW	47	—	D-GND	72	O	CCLP	97	I	WD1
23	O	HAF	48	O	WZR	73	O	IDW	98	I	SCH
24	O	BF0	49	O	RZR	74	O	FPO1	99	I	NRE
25	O	PED	50	O	RCK	75	O	FPO2	100	I	CDC


67
68
X1
X2
87 A-TEST
88 D-TEST
40 NS0
39 NS1
38 NS2
16 BC1
93 BC2
12 BST
100 CDC
8 CDO
55 CRF
69 DATA
51 DRC
53 DRZ
76 FPI1
77 FPI2
31 LLT
45 MD1
44 MD2
43 MD3
42 MD4
11 NRA
99 NRE
13 PCR
29 PH0
30 PH1
15 RH1
95 RH2
5 RH3
14 RL1
94 RL2
6 RL3
98 SCH
71 SCLK
82 SD0
81 SD1
80 SD2
70 STB
64 STD
9 V1A
10 V2A
2 V1E
1 V2E
28 WCK
97 WD1
96 WD2
7 YDO
37 ACP
24 BF0
33 BPF
22 BW
36 CBLK
72 CCLP
84 CHS
32 COL
59 CRFS
21 CSY1
86 CSY2
79 ECDO
78 EYDO
74 FPO1
75 FPO2
83 FPR
23 HAF
34 HBLK
85 HLD
63 HLFH
73 IDW
62 LN12
60 O/E
25 PED
52 RC1
50 RCK
54 RZ1
49 RZR
26 SMP
27 STUP
61 SVRF
35 VISC
48 WZR
57 YBLK
56 YCLP
58 YRFS
RST
41

INPUT

A-TEST	;	ANALOG NODE TEST
BC1, BC2	;	BIAS CURRENT
BST	;	BURST
CDC	;	SLICE LEVEL
CDO	;	C DROPOUT PULSE
CLR	;	RESET (L : RESET)
CRF	;	EXTERNAL C-REFERENCE SYNC
DATA	;	SERIAL DATA
DRC	;	32 nSec DELAYED READ CLOCK (PAL ONLY)
DRZ	;	100 nSec DELAYED READ CLOCK
D-TEST	;	DIGITAL MODE TEST
FPI1, FPI2	;	DETECTED COLOR FRAME ID
LLT	;	LALT
MD1, MD2	;	VIDEO MODE SELECT
MD3, MD4	;	SIGNAL MODE SELECT
NRA	;	INTEGRATOR FOR REJECTING THE SPIKE NOISE ON THE SEPARATED SYNC
NRE	;	INTEGRATOR FOR REJECTING THE SPIKE NOISE ON THE SEPARATED SYNC
NS0 - NS2	;	TEST SIGNAL FOR THE DIGITAL TEST MODE
PCR	;	EXTERNAL CR FOR DESIGNATING THE SAMPLING PULSE WIDTH
PH0	;	1/2 WCK (2 fsc)
PH1	;	1/4 WCK (fsc)
RH1 - RH3	;	REFERENCE VOLTAGE (+1.8 V)
RL1 - RL3	;	REFERENCE VOLTAGE (+1.7 V)
SCH	;	DETECTED SC/H VOLTAGE
SCLK	;	SERIAL DATA CLOCK
SD0 - SD2	;	COLOR FRAMING PHASE ADJUSTMENT
STB	;	SERIAL DATA STROBE
STD	;	STANDARD MODE SIGNAL FROM THE SYSTEM CONTROLLER
V1A	;	VIDEO SIGNAL FOR CLAMP PULSE GENERATION
V2A	;	VIDEO SIGNAL FOR SYNC SEPARATION
V1E	;	SELECT Y SIGNAL FOR CLAMP PULSE GENERATION
V2E	;	SELECT Y SIGNAL FOR SYNC SEPARATION
WCK	;	WRITE CLOCK (4 fsc)
WD1	;	LOWER WINDOW VOLTAGE FOR THE COLOR FRAMING DETECTOR
WD2	;	UPPER WINDOW VOLTAGE FOR THE COLOR FRAMING DETECTOR
X1	;	EXTERNAL CRYSTAL OSCILLATOR
YDO	;	Y DROPOUT PULSE

OUTPUT

ACP	;	SYNC-TIP CLAMP PULSE
BF0	;	BURST GATE PULSE
BPF	;	L : BAND-PASS FILTER MODE PERIOD
BW	;	H : B/W, L : COLOR
CBLK	;	BLANKING
CCLP	;	CTDM CLAMP PULSE
CHS	;	CHARGE START OF COLOR FRAMING DETECTION
COL	;	H : COLOR PERIOD, L : B/W PERIOD (ALWAYS “H” IN S-VIDEO MODE)
CRFS	;	C REFERENCE SYNC GENERATION SIGNAL
CSY1, CSY2	;	SEPARATED SYNC
ECDO	;	C DROPOUT
EYDO	;	Y DROPOUT
FPO1	;	FP1 OR CTDM FP1 OUTPUT
FPO2	;	FP2 OR CTDM FP2 OUTPUT
FPR	;	FIELD PULSE GENERATOR RESET PULSE
HAF	;	HALF H PULSE
HBLK	;	H SYNC TIMING PULSE
HLD	;	SAMPLING PULSE FOR THE COLOR FRAMING DETECTOR
HLFH	;	FRONT HALF AND BACK HALF OF EACH LINE (L : FRONT HALF)
IDW	;	CTDM CF-ID WINDOW
LN12	;	L : 12 LINES PERIOD
O/E	;	ODD/EVEN (H : EVEN, L : ODD)
PED	;	PEDESTAL SAMPLING PULSE
RC1	;	READ CLOCK FOR DELAYING IT FOR 35 ns
RCK	;	READ CLOCK
RZ1	;	READ CLOCK FOR DELAYING IT FOR 100 ns
RZR	;	READ ZERO
SMP	;	SAMPLING PULSE
STUP	;	CAV Y SETUP PULSE
SVRF	;	SERVO REFERENCE
VISC	;	SYSTEM CONTROLLER OPERATION STATUS
WZR	;	WRITE ZERO
X2	;	EXTERNAL CRYSTAL OSCILLATOR
YBLK	;	Y BLANKING PULSE
YCLP	;	SELECT Y CLAMP
YRFS	;	Y REFERENCE SYNC GENERATION SIGNAL