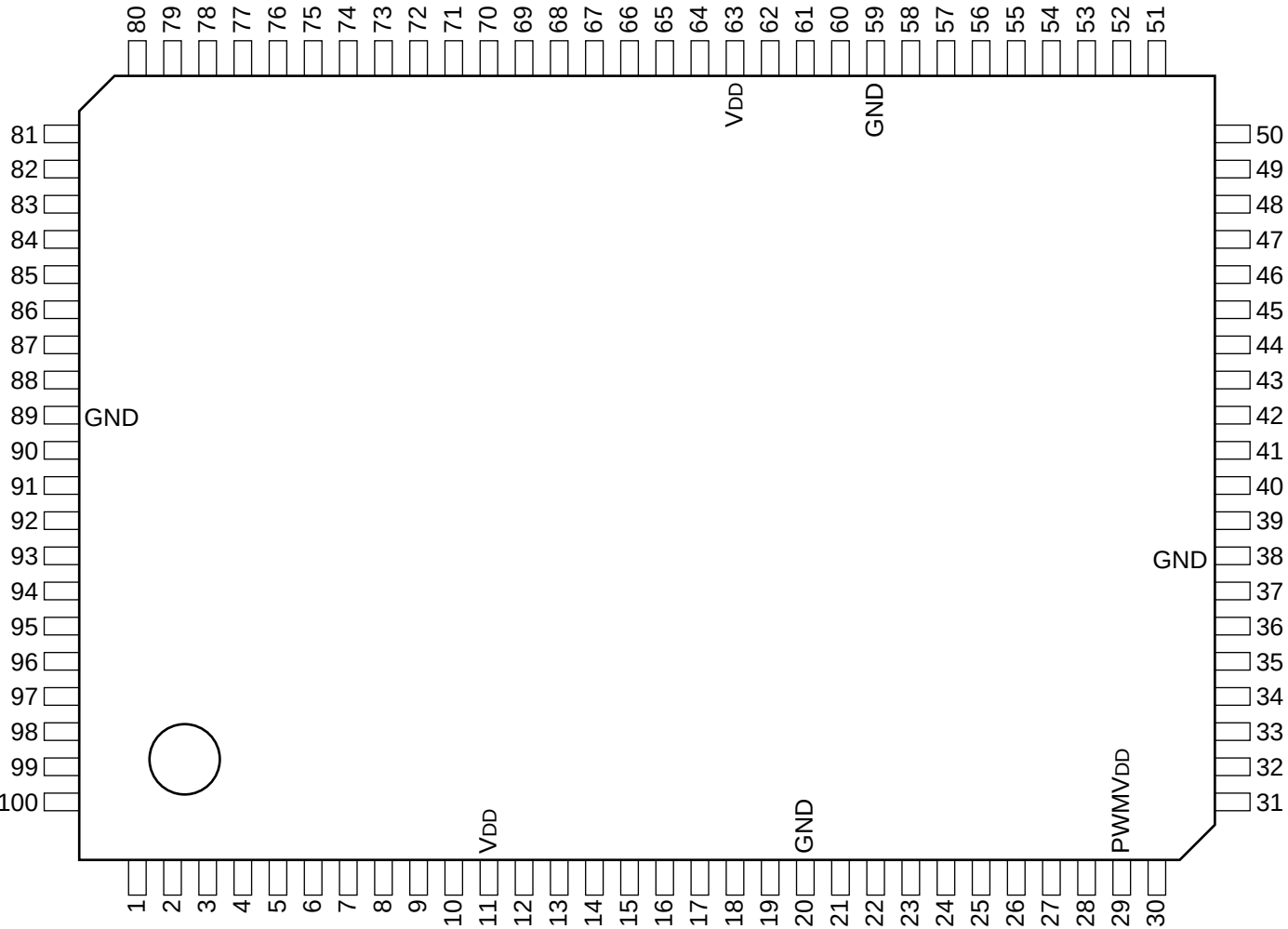


SERVO IC

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	FG1/IP24	26	I/O	IOP2	51	I/O	D7	76	O	PPG11/OP21
2	I	FG0/IP23	27	I/O	IOP1	52	I/O	D6	77	O	PPG10/OP20
3	I	PBH/IP22	28	I/O	IOP0	53	I/O	D5	78	O	PPG0F/OP17
4	I	SYNC1/IP21	29	—	PWM V _{DD}	54	I/O	D4	79	O	PPG0E/OP16
5	I	SYNC0/IP20	30	O	PWM7/OP37	55	I/O	D3	80	O	PPG0D/OP15
6	I	FG02/IP14	31	O	PWM6/OP36	56	I/O	D2	81	O	PPG0C/OP14
7	I	FG01/IP13	32	O	PWM5/OP35	57	I/O	D1	82	O	PPG0B/OP13
8	I	FG00/IP12	33	O	PWM4/OP34	58	I/O	D0	83	O	PPG0A/OP12
9	I	CTL/IP11	34	O	PWM3/OP33	59	—	GND	84	O	PPG09/OP11
10	I	LAT/IP10	35	O	PWM2/OP32	60	I	RES	85	O	PPG08/OP10
11	—	V _{DD}	36	O	PWM1/OP31	61	I	MD1	86	O	CLKO
12	I	UD/IP07	37	O	PWM0/OP30	62	I	MD0	87	I	EXTAL
13	I	CCLK/IP06	38	—	GND	63	—	V _{DD}	88	O	XTAL
14	I	FGC1/IP05	39	I	AS14	64	I	WR	89	—	GND
15	I	FGC0/IP04	40	I	AS13	65	I	RD	90	O	PPG07/OP07
16	I	FGB1/IP03	41	I	A15	66	I	CE	91	O	PPG06/OP06
17	I	FGB0/IP02	42	I	A14	67	O	IREQ2	92	O	PPG05/OP05
18	I	FGA1/IP01	43	I	A13	68	O	IREQ1	93	O	PPG04/OP04
19	I	FGA0/IP00	44	I	A6	69	O	IREQ0	94	O	PPG03/OP03
20	—	GND	45	I	A5	70	I	FXSEL	95	O	PPG02/OP02
21	I/O	IOP7	46	I	A4	71	O	OP26	96	O	PPG01/OP01
22	I/O	IOP6	47	I	A3	72	O	EXCS1/OP25	97	O	PPG00/OP00
23	I/O	IOP5	48	I	A2	73	O	EXCS0/OP24	98	I	FG12/IP27
24	I/O	IOP4	49	I	A1	74	O	PPG13/OP23	99	I	FG11/IP26
25	I/O	IOP3	50	I	A0	75	O	PPG12/OP22	100	I	FG10/IP25

41	A15	D7	51	INPUT	
42	A14	D6	52	A0 - A15	; ADDRESS BUS
43	A13	D5	53	AS13, AS14	; SELECTING CONDITION OF ADDRESS DECODER AS13 AND AS14 BITS
44	A6	D4	54	CCLK	; 8-BIT COUNTER CLOCK INPUT
45	A5	D3	55	CE	; CHIP ENABLE
46	A4	D2	56	CTL	; RESOLUTION 2.5MHz WITH EDGE SELECT FUNCTION.
47	A3	D1	57		WITH FREQUENCY DIVISION MASK TIMER
48	A2	D0	58	EXTAL	; CRYSTAL OSCILLATION OR EXTERNAL CLOCK INPUT
49	A1			FG0	; RESOLUTION 2.5MHz
50	A0	IOP7	21	FG00 - FG02	; FREQUENCY DIVISION ENABLE RESOLUTION 2.5MHz.
		IOP6	22		WITH FREQUENCY DIVISION MASK TIMER
39	AS14	IOP5	23	FG1	; RESOLUTION 2.5MHz BOTH EDGES
40	AS13	IOP4	24	FG10	; EDGE SELECTION ENABLE RESOLUTION 10MHz
		IOP3	25	FG11, FG12	; FREQUENCY DIVISION ENABLE RESOLUTION 10MHz
98	FG12/IP27	IOP2	26	FGA0	; PERFORMS FORWARD/REVERSE ROTATION DETECTION
99	FG11/IP26	IOP1	27		AND 4FG COUNT (UP/DOWN) BY FGA0 AND FGA1. 10BITS. UP/DOWN IS MADE BY
100	FG10/IP25	IOP0	28		CONTROLLING THE UP/DOWN OF 8-BIT COUNTER.
6	FG02/IP14			FGA1	; 4FG PERFORMS FREQUENCY DIVISION AND FRC CAPTURE
7	FG01/IP13	PWM7/OP37	30		THROUGH MASK TIMER.
8	FG00/IP12	PWM6/OP36	31		*1 : SELECTS ONE OF FGA0 TO FGC1 INPUT AND DETECTS
1	FG1/IP24	PWM5/OP35	32		BOTH EDGES AND PERFORM THE FRC CAPTURE THROUGH
2	FG0/IP23	PWM4/OP34	33	FGB0	THE MASK TIMER.
		PWM3/OP33	34		PERFORMS FORWARD/REVERSE ROTATION DETECTION AND 4FG COUNT
4	SYNCl/IP21	PWM2/OP32	35		BY FGB0 AND FGB1.
5	SYNCO/IP20	PWM1/OP31	36	FGB1	; *1 : SELECTS ONE OF FGA0 TO FGC1 INPUT AND DETECTS
		PWM0/OP30	37		BOTH EDGES AND PERFORM THE FRC CAPTURE THROUGH
3	PBH/IP22				THE MASK TIMER.
		PPG0F/OP17	78	FGC0	; PERFORMS FORWARD/REVERSE ROTATION DETECTION AND 4FG COUNT
9	CTL/IP11	PPG0E/OP16	79		BY FGC0 AND FGC1.
10	LAT/IP10	PPG0D/OP15	80	FGC1	; *1 : SELECTS ONE OF FGA0 TO FGC1 INPUT AND DETECTS
12	UD/IP07	PPG0C/OP14	81		BOTH EDGES AND PERFORM THE FRC CAPTURE THROUGH
13	CCLK/IP06	PPG0B/OP13	82		THE MASK TIMER.
		PPG0A/OP12	83	FXSEL	; FREQUENCY DIVISION SELECTION CLOCK INPUT
14	FGC1/IP05	PPG13/OP23	74	LAT	; EXTERNAL LATCH TIMING OF UP/DOWN COUNTER
15	FGC0/IP04	PPG12/OP22	75	MD0, 1	; TEST MODE DESIGNATION
16	FGB1/IP03	PPG11/OP21	76	PBH	; INPUT OF COMPOSITE SYNC OR H SYNC.
17	FGB0/IP02	PPG10/OP20	77		RESOLUTION 10MHz. WITH HALF H KILLER.
18	FGA1/IP01	PPG09/OP11	84	RD	; REDE
19	FGA0/IP00	PPG08/OP10	85	RES	; RESET
				SYNCO, 1	; INPUT OF COMPOSITE SYNC OR V SYNC. RESOLUTION 2.5MHz
61	MD1	PPG07/OP07	90	UD	; 8-BIT COUNTER UP/ DOWN INPUT
62	MD0	PPG06/OP06	91	WR	; WRITE
60	RES	PPG05/OP05	92		
70	FXSEL	PPG04/OP04	93	OUTPUT	
87	EXTAL	PPG03/OP03	94	CLKO	; CLOCK OUTPUT
		PPG02/OP02	95	EXCS0, 1	; DECODE AT ADDRESS A3 LEVEL
		PPG01/OP01	96	IREQ0	; INTERRUPTION SIGNAL OF FRC CAPTURE UNIT
		PPG00/OP00	97	IREQ1	; COINCIDENCE INTERRUPTION OF PPG0
				IREQ2	; COINCIDENCE INTERRUPTION OF PPG1
				OP26	; EXCLUSIVELY OUTPUT PORT
		OP26	71	PPG00 - PPG0F	
		EXCS1/OP25	72	PPG10 - PPG13	; PROGRAMMABLE PULSE GENERATOR RESOLUTION 1.25MHz
		EXCS0/OP24	73		PPG00 : WITH HLOCK
				PWM0 - PWM5	; PWM OUTPUT NORMALLY PWM, OR PWM0 AND PWM1, PWM2 AND PWM3,
					OR PWM4 AND PWM5 OUTPUT SIGNAL CORRESPONDED TO PUSH-PULL.
		IREQ2	67	PWM6, 7	; PWM OUTPUT
		IREQ1	68	XTAL	; CRYSTAL OSCILLATION
		IREQ0	69		
				INPUT/OUTPUT	
		CLKO	86	D0 - D7	; DATA BUS
		XTAL	88	IOP0 - IOP7	; SELECTS AND USES INPUT AND OUTPUT BY EVERY 1 BIT.

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