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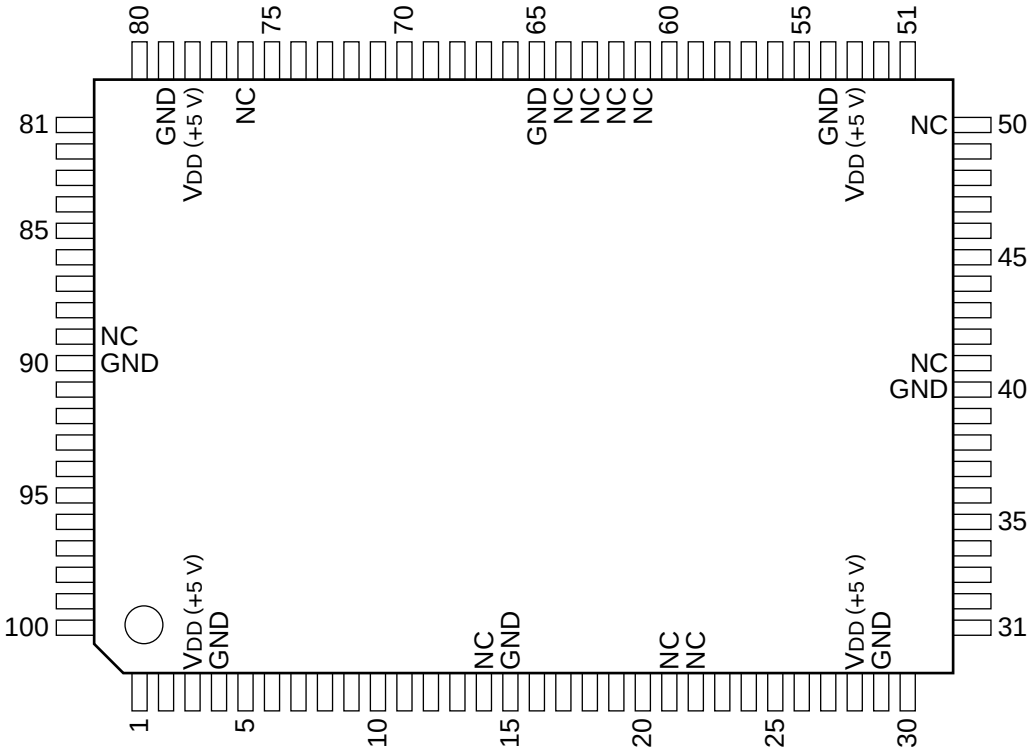
# C-MOS GATE ARRAY

—TOP VIEW—




($V_{DD}$ = +5 V)

| PIN No. | I/O | SIGNAL | PIN No. | I/O | SIGNAL | PIN No. | I/O | SIGNAL | PIN No. | I/O | SIGNAL | PIN No. | I/O | SIGNAL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | I | DA0 | 21 | — | NC | 41 | — | NC | 61 | — | NC | 81 | I | GI2 |
| 2 | I | DA1 | 22 | — | NC | 42 | O | GO0 | 62 | — | NC | 82 | I | GI3 |
| 3 | — | $V_{DD}$ | 23 | — | TCK | 43 | O | GO1 | 63 | — | NC | 83 | I | GI4 |
| 4 | — | GND | 24 | — | TDI | 44 | O | GO2 | 64 | — | NC | 84 | I | GI5 |
| 5 | I | DA2 | 25 | — | TENA1 | 45 | O | GO3 | 65 | — | GND | 85 | I | GI6 |
| 6 | I | DA3 | 26 | — | TD0 | 46 | O | GO4 | 66 | I | BI0 | 86 | I | GI7 |
| 7 | I | DA4 | 27 | — | VDT | 47 | O | GO5 | 67 | I | BI1 | 87 | I | GI8 |
| 8 | I | DA5 | 28 | — | $V_{DD}$ | 48 | O | GO6 | 68 | I | BI2 | 88 | I | GI9 |
| 9 | I | AD0 | 29 | — | GND | 49 | O | GO7 | 69 | I | BI3 | 89 | — | NC |
| 10 | I | AD1 | 30 | — | CK | 50 | — | NC | 70 | I | BI4 | 90 | — | GND |
| 11 | I | AD3 | 31 | I | RST | 51 | O | RO0 | 71 | I | BI5 | 91 | I | RI0 |
| 12 | I | CS | 32 | I | BO0 | 52 | O | RO1 | 72 | I | BI6 | 92 | I | RI1 |
| 13 | I | WR | 33 | O | BO1 | 53 | — | $V_{DD}$ | 73 | I | BI7 | 93 | I | RI2 |
| 14 | — | NC | 34 | O | BO2 | 54 | — | GND | 74 | I | BI8 | 94 | I | RI3 |
| 15 | — | GND | 35 | O | BO3 | 55 | O | RO2 | 75 | I | BI9 | 95 | I | RI4 |
| 16 | I | MX0 | 36 | O | BO4 | 56 | O | RO3 | 76 | — | NC | 96 | I | RI5 |
| 17 | I | MX1 | 37 | O | BO5 | 57 | O | RO4 | 77 | I | GI0 | 97 | I | RI6 |
| 18 | I | UV | 38 | O | BO6 | 58 | O | RO5 | 78 | — | $V_{DD}$ | 98 | I | RI7 |
| 19 | I | EHK | 39 | O | BO7 | 59 | O | RO6 | 79 | — | GND | 99 | I | RI8 |
| 20 | I | P4 | 40 | O | GND | 60 | O | RO7 | 80 | I | GI1 | 100 | I | RI9 |