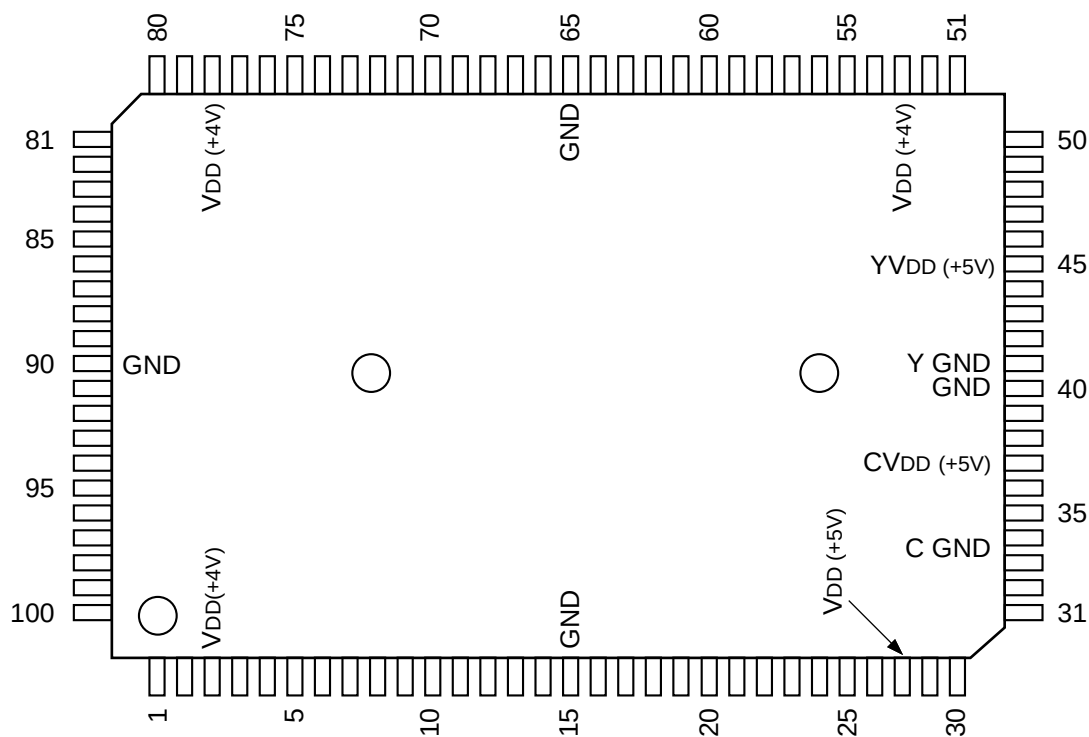

C-MOS Y/C SEPARATOR

—TOP VIEW—



(VDD = +4V/CVDD, YVDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	FV11	21	I	TST2	41	—	Y GND	61	I	SCL	81	O	VRR1
2	I	FV28	22	O	DC0	42	O	AYO	62	I	SDA	82	O	VRR2
3	—	VDD	23	O	DC1	43	O	YVG	63	I	VP	83	O	VRR3
4	I	FV27	24	O	DC2	44	I	YVRF	64	I	VIN8	84	O	LVO8
5	I	FV26	25	O	DC3	45	—	YVDD	65	—	GND	85	O	LVO7
6	I	FV25	26	O	DC4	46	O	YIRF	66	I	VIN7	86	O	LVO6
7	I	FV24	27	O	DC5	47	O	YVB	67	I	VIN6	87	O	LVO5
8	I	FV23	28	—	VDD	48	I	POR	68	I	VIN5	88	O	LVO4
9	I	FV22	29	O	DC6	49	O	DY9	69	I	VIN4	89	O	LVO3
10	I	FV21	30	O	DC7	50	O	DY8	70	I	VIN3	90	—	GND
11	I	FV20	31	O	DC8	51	O	DY7	71	I	VIN2	91	O	LVO2
12	O	MO1	32	O	DC9	52	O	DY6	72	I	VIN1	92	O	LVO1
13	O	MO0	33	—	C GND	53	—	VDD	73	I	VIN0	93	O	LVO0
14	I	MI1	34	O	ACO	54	O	DY5	74	I	TST4	94	I	FV18
15	—	GND	35	O	CVG	55	O	DY4	75	I	CKI2	95	I	FV17
16	I	MI0	36	I	CVRF	56	O	DY3	76	O	CKO	96	I	FV16
17	O	MDO	37	—	CVDD	57	O	DY2	77	I	CKI1	97	I	FV15
18	I	MDF1	38	O	CIRF	58	O	DY1	78	—	VDD	98	I	FV14
19	I	MDF2	39	O	CVB	59	O	DY0	79	I	BGP	99	I	FV13
20	I	TST1	40	—	GND	60	I	TST3	80	O	VRW	100	I	FV12

2	FV28	DC9	32
4	FV27	DC8	31
5	FV26	DC7	30
6	FV25	DC6	29
7	FV24	DC5	27
8	FV23	DC4	26
9	FV22	DC3	25
10	FV21	DC2	24
11	FV20	DC1	23
		DC0	22
94	FV18		
95	FV17	DY9	49
96	FV16	DY8	50
97	FV15	DY7	51
98	FV14	DY6	52
99	FV13	DY5	54
100	FV12	DY4	55
1	FV11	DY3	56
		DY2	57
64	VIN8	DY1	58
66	VIN7	DY0	59
67	VIN6		
68	VIN5	LVO8	84
69	VIN4	LVO7	85
70	VIN3	LVO6	86
71	VIN2	LVO5	87
72	VIN1	LVO4	88
73	VIN0	LVO3	89
		LVO2	91
14	MI1	LVO1	92
16	MI0	LVO0	93
62	SDA	ACO	34
61	SCL	AYO	42
77	CKI1	MO1	12
75	CKI2	MO0	13
		MDO	17
18	MDF1		
19	MDF2	CVG	35
		CIRF	38
20	TST1	CVB	39
21	TST2	YVG	43
60	TST3	YIRF	46
74	TST4	YVB	47
48	POR	CKO	76
63	VP	VRW	80
79	BGP	VRR1	81
36	CVRF	VRR2	82
44	YVRF	VRR3	83

INPUT

BGP	; BURST GATE PULSE
CKI1	; SYSTEM CLOCK
CKI2	; CXD2029Q MASTER CLOCK (=CKO)
CVRF	; ANALOG CHROMA V REFERENCE
FV11 - FV18	; FRAME DELAY (525H)
FV20 - FV28	; FRAME DELAY (526H)
MDF1, MDF2	; TEMPORAL FILTER
MI0, MI1	; CHROMA 2 FRAME DELAY
POR	; IIC BUS POWER ON RESET
SCL	; IIC BUS CLOCK
SDA	; IIC BUS DATA
TST1 - TST4	; TEST PIN (NORMAL USE IS LOW)
VIN0 - VIN8	; DIGITAL COMPOSITE VIDEO
VP	; V PULSE
YVRF	; ANALOG LUMINANCE V REFERENCE

OUTPUT

ACO	; ANALOG CHROMA
AYO	; ANALOG LUMINANCE
CIRF	; CONNECT 16 TIMES OUTPUT RESISTANCE
CKO	; SYSTEM CLOCK
CVB, CVG	; CONNECT ABOUT 0.1μF
DC0 - DC9	; DIGITAL CHROMA
DY0 - DY9	; DIGITAL LUMINANCE
LVO0 - LVO8	; 2H DELEY
MDO	; TEMPORAL FILTER
MO0, MO1	; CHROMA 1 FRAME DELAY
VRR1 - VRR3	; V READ RESET
VRW	; V WIGHT RESET
YIRF	; CONNECT 16 TIMES OUTPUT RESISTANCE
YVB, YVG	; CONNECT ABOUT 0.1μF

