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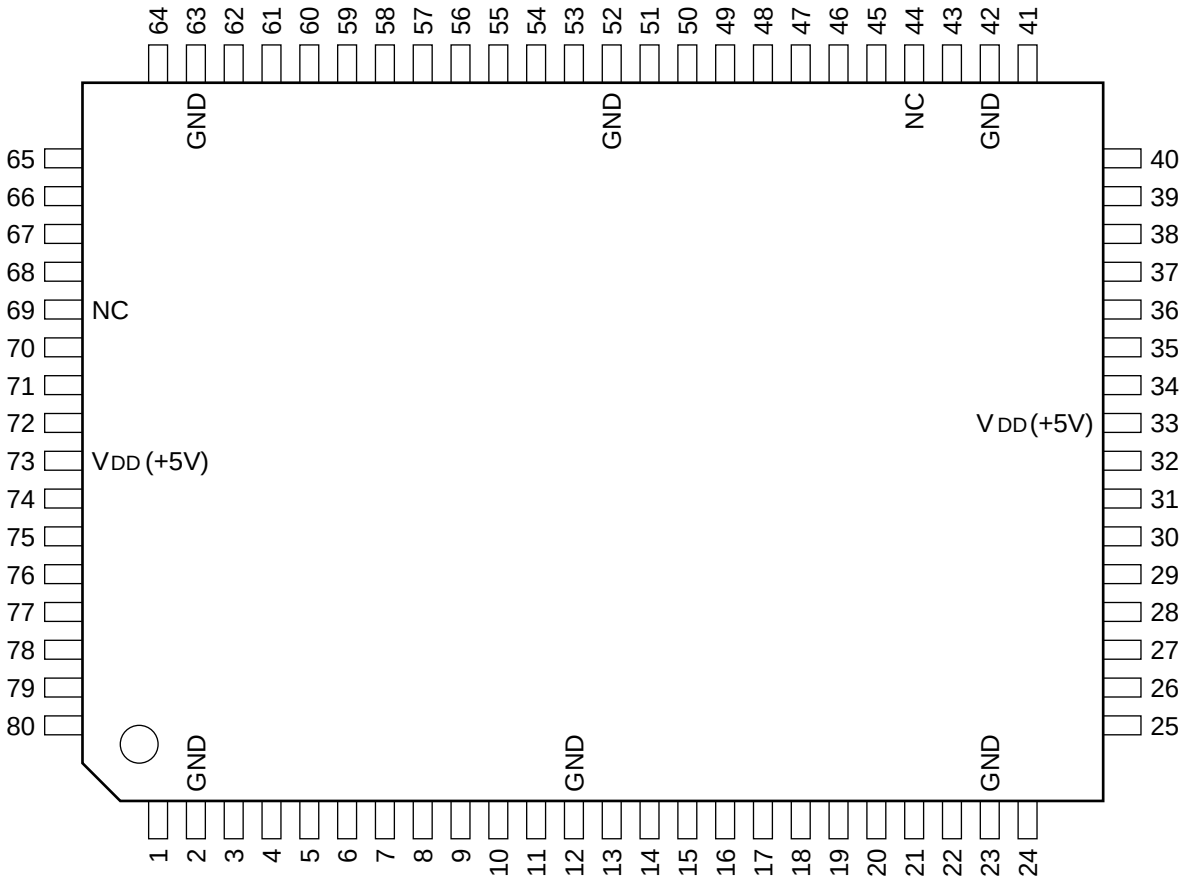
IL08

C-MOS Y/C INTERPOLATION FOR DIGITAL FRAME MEMORY TV

- TOP VIEW -



(V_{DD} =+5V)

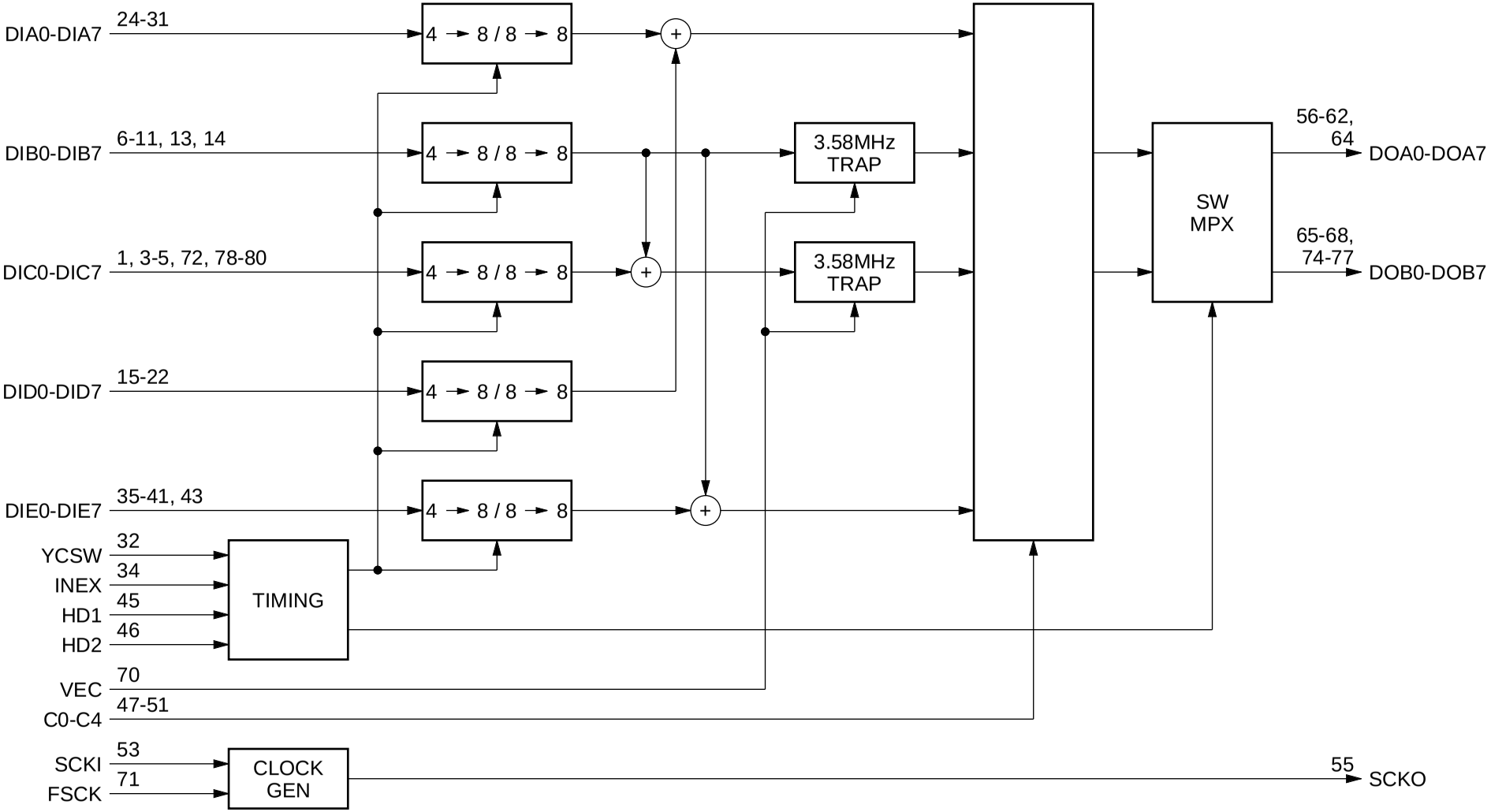
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	DIC3	21	I	DID1	41	I	DIE1	61	O	DOA5
2	–	GND	22	I	DID0	42	–	GND	62	O	DOA6
3	I	DIC2	23	–	GND	43	I	DIE0	63	–	GND
4	I	DIC1	24	I	DIA7	44	–	NC	64	O	DOA7
5	I	DIC0	25	I	DIA6	45	I	HD1	65	O	DOB0
6	I	DIB7	26	I	DIA5	46	I	HD2	66	O	DOB1
7	I	DIB6	27	I	DIA4	47	I	C4	67	O	DOB2
8	I	DIB5	28	I	DIA3	48	I	C3	68	O	DOB3
9	I	DIB4	29	I	DIA2	49	I	C2	69	–	NC
10	I	DIB3	30	I	DIA1	50	I	C1	70	I	VEC
11	I	DIB2	31	I	DIA0	51	I	C0	71	I	FSCK
12	–	GND	32	I	YCSW	52	–	GND	72	I	DIC7
13	I	DIB1	33	–	V_{DD}	53	I	SCKI	73	–	V_{DD}
14	I	DIB0	34	I	INEX	54	I	POR	74	O	DOB4
15	I	DID7	35	I	DIE7	55	O	SCK0	75	O	DOB5
16	I	DID6	36	I	DIE6	56	O	DOA0	76	O	DOB6
17	I	DID5	37	I	DIE5	57	O	DOA1	77	O	DOB7
18	I	DID4	38	I	DIE4	58	O	DOA2	78	I	DIC6
19	I	DID3	39	I	DIE3	59	O	DOA3	79	I	DIC5
20	I	DID2	40	I	DIE2	60	O	DOA4	80	I	DIC4

INPUT

C0-C4	; MOTION COMPENSATION CONTROL SIGNAL
DIA0-DIA7	; VIDEO ORIGINAL SIGNAL
DIB0-DIB7	; 262H DELAYED SIGNAL FROM VIDEO ORIGINAL SIGNAL
DIC0-DIC7	; 263H DELAYED SIGNAL FROM VIDEO ORIGINAL SIGNAL
DID0-DID7	; 525H DELAYED SIGNAL FROM VIDEO ORIGINAL SIGNAL
DIE0-DIE7	; 787H DELAYED SIGNAL FROM VIDEO ORIGINAL SIGNAL
FSCK	; 28.6MHz CLOCK
HD1, HD2	; INTERNAL REFERENCE H SIGNAL
INEX	; SAMPLING FREQUENCY SELECT SIGNAL FOR COLOR DIFFERENCE SIGNAL (H : 4:1:1, L : 4:2:2)
POR	; TEST (NORMAL : H)
SCKI	; 14.3MHz CLOCK
VEC	; 3.58MHz TRAP FILTER ON/OFF CONTROL SIGNAL
YCSW	; Y/C-Y SELECT (H:Y, L:C-Y)

OUTPUT

DOA0-DOA7	; Y SIGNAL / R-Y SIGNAL (WHEN THE YCSW IS H:Y SIGNAL, WHEN THE YCSW IS L:R-Y SIGNAL)
DOB0-DOB7	; B-Y SIGNAL (WHEN THE YCSW IS L)
SCK0	; 14.3MHz CLOCK


DIA0-DIA7
24-31
DIB0-DIB7
6-11, 13, 14
DIC0-DIC7
1, 3-5, 72, 78-80
DID0-DID7
15-22
DIE0-DIE7
35-41, 43
4 → 8 / 8 → 8
3.58MHz TRAP
3.58MHz TRAP
SW MPX
56-62, 64
DOA0-DOA7
65-68, 74-77
DOB0-DOB7
YCSW
32
INEX
34
HD1
45
HD2
46
TIMING
VEC
70
C0-C4
47-51
SCKI
53
FSCK
71
CLOCK GEN
55
SCKO
CXD2004Q (4/4)