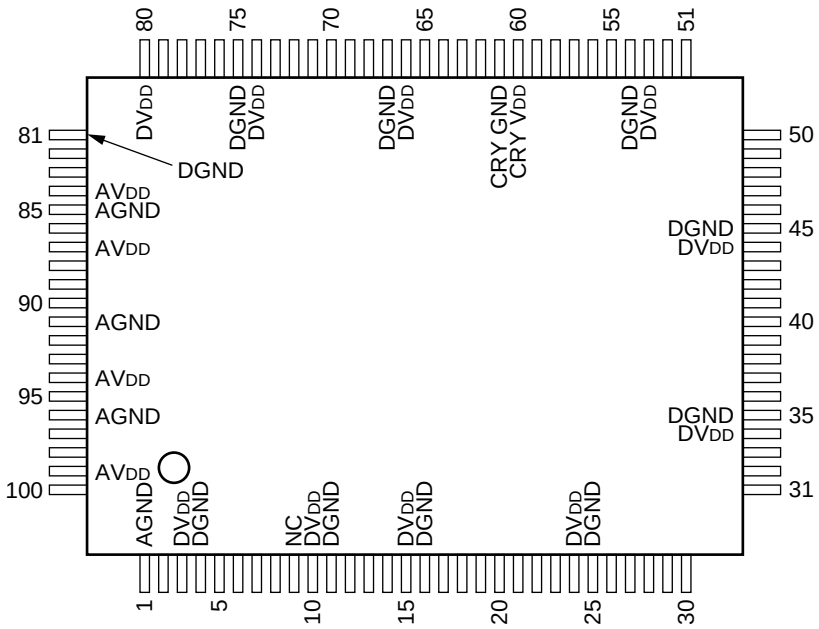
C-MOS QPSK DEMODULATOR AND FORWARD ERROR CORRECTION

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	AGND	26	O	PKTCLK	51	I	TEST18	76	O	CR4
2	I	RB0	27	O	BYTCLK	52	I	TEST19	77	O	CR5
3	—	DV_{DD}	28	O	PKTERR	53	—	DV_{DD}	78	O	CR6
4	—	DGND	29	O	DATA0	54	—	DGND	79	O	CR7
5	I	TEST1	30	O	DATA1	55	I	TEST20	80	—	DV_{DD}
6	I	TEST2	31	O	DATA2	56	I	TEST21	81	—	DGND
7	I	TEST3	32	O	DATA3	57	I	TEST22	82	O	QSYNC
8	I	TEST4	33	O	DATA4	58	I	SCL	83	O	FSYNC
9	—	NC	34	—	DV_{DD}	59	I/O	SDA	84	—	AV_{DD}
10	—	DV_{DD}	35	—	DGND	60	—	CRY V_{DD}	85	—	AGND
11	—	DGND	36	O	DATA5	61	—	CRY GND	86	O	CPOUT
12	O	SDATA/SCL	37	O	DATA6	62	O	XO	87	—	AV_{DD}
13	O	SCLK	38	O	DATA7	63	I	XI	88	I	VCOC
14	I/O	SEN/SDA	39	I/O	TEST8	64	O	VDT	89	I	OPXIN
15	—	DV_{DD}	40	I/O	TEST9	65	O	VCK	90	O	OPOUT
16	—	DGND	41	I/O	TEST10	66	—	DV_{DD}	91	—	AGND
17	I	TCK	42	I/O	TEST11	67	—	DGND	92	I	VCOEN
18	I	TMS	43	I/O	TEST12	68	O	AGCPWM	93	I	RT1
19	I	TEST6	44	—	DV_{DD}	69	O	CKV	94	—	AV_{DD}
20	I	TEST7	45	—	DGND	70	O	CR0	95	I	QIN
21	O	CK8OUT	46	I/O	TEST13	71	O	CR1	96	—	AGND
22	I	RESET	47	I/O	TEST14	72	O	CR2	97	I	RB1
23	I	TE	48	I/O	TEST15	73	O	CR3	98	I	RT0
24	—	DV_{DD}	49	I	TEST16	74	—	DV_{DD}	99	—	AV_{DD}
25	—	DGND	50	I	TEST17	75	—	DGND	100	I	IIN

INPUT

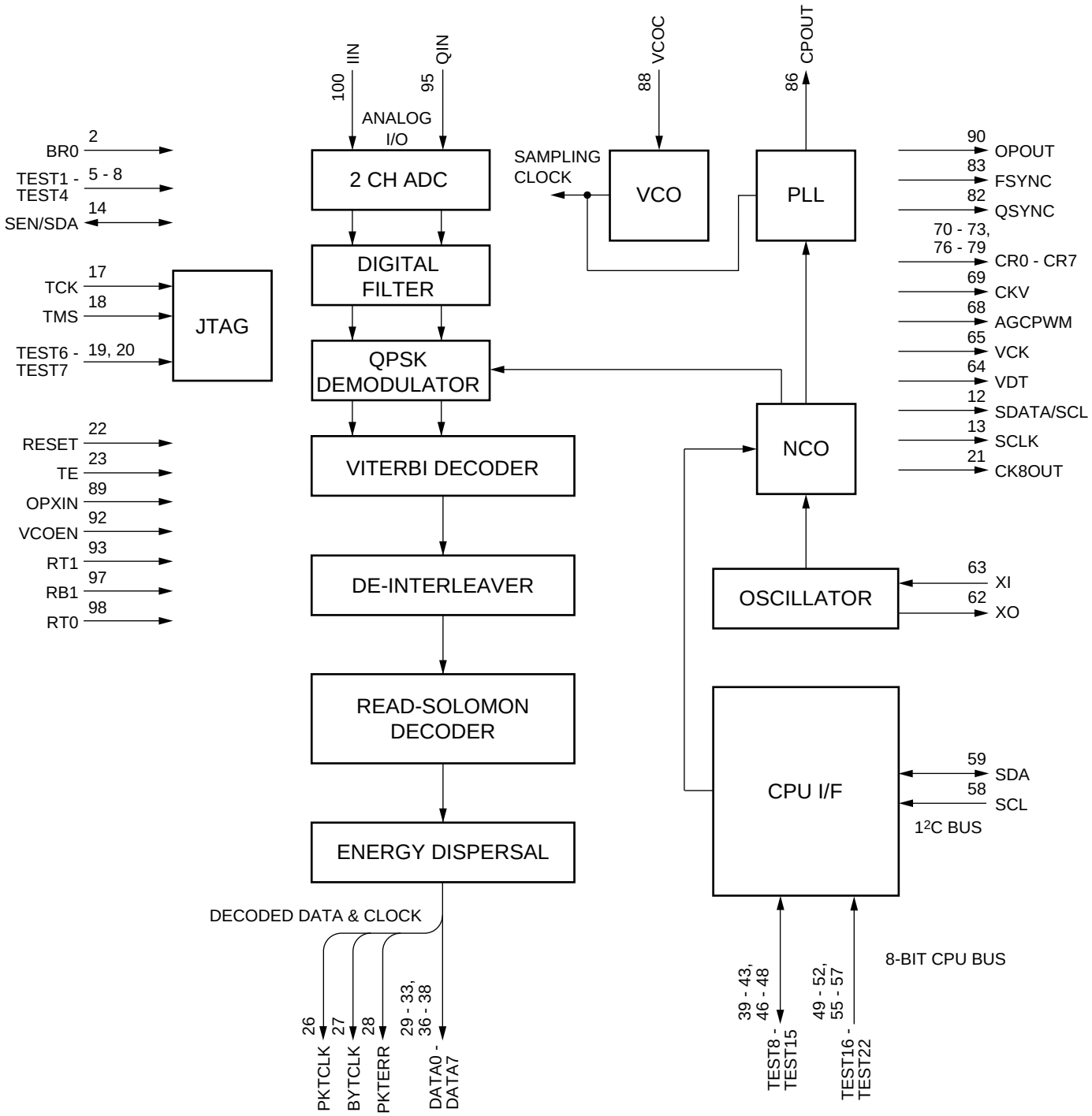
IIN	:	I SIGNAL
OPXIN	:	OP AMP
QIN	:	Q SIGNAL
RB0, RB1	:	BOTTOM REFERENCE VOLTAGE
RESET	:	RESET
RT0, RT1	:	TOP REFERENCE VOLTAGE
SCL	:	I^2C CLOCK
TCK	:	TEST CLOCK
TE	:	TEST ENABLE
TEST1 - TEST7	:	TEST
TEST16 - TEST22	:	TEST
TMS	:	TEST
VCOC	:	VCO CONTROL
VCOEN	:	VCO ENABLE
XI	:	OSCILLATOR

OUTPUT

AGCPWM	:	AGC PWM
BYTCLK	:	DATA CLOCK
CK8OUT	:	CLOCK (1/8)
CKV	:	SYMBOL CLOCK
CPOUT	:	CHARGE PUMP
CR0 - CR7	:	CLOCK
DATA0 - DATA7	:	DATA
OPOUT	:	OP AMP
PKTCLK	:	PACKET CLOCK
PKTERR	:	PACKET ERROR
QSYNC	:	CARRIER LOCK
FSYNC	:	FRAME LOCK
SCLK	:	SERIAL CLOCK
SDATA/SCL	:	SERIAL DATA
VCK	:	VITERBI CLOCK
VDT	:	VITERBI DATA
XO	:	OSCILLATOR

INPUT/OUTPUT

SDA	:	I^2C DATA
SEN/SDA	:	SERIAL ENABLE
TEST8 - TEST15	:	TEST


100 IIN
95 QIN
ANALOG I/O
88 VCOC
86 CPOUT
2 CH ADC
SAMPLING CLOCK
VCO
PLL
DIGITAL FILTER
QPSK DEMODULATOR
VITERBI DECODER
DE-INTERLEAVER
READ-SOLOMON DECODER
ENERGY DISPERSAL
NCO
OSCILLATOR
CPU I/F
JTAG
BR0 2
TEST1 - TEST4 5 - 8
SEN/SDA 14
TCK 17
TMS 18
TEST6 - TEST7 19, 20
RESET 22
TE 23
OPXIN 89
VCOEN 92
RT1 93
RB1 97
RT0 98
90 OPOUT
83 FSYNC
82 QSYNC
70 - 73, 76 - 79 CR0 - CR7
69 CKV
68 AGCPWM
65 VCK
64 VDT
12 SDATA/SCL
13 SCLK
21 CK8OUT
63 XI
62 XO
59 SDA
58 SCL
I²C BUS
8-BIT CPU BUS
39 - 43, 46 - 48 TEST8 - TEST15
49 - 52, 55 - 57 TEST16 - TEST22
DECODED DATA & CLOCK
26 PKTCLK
27 BYTCLK
28 PKTERR
29 - 33, 36 - 38 DATA0 - DATA7