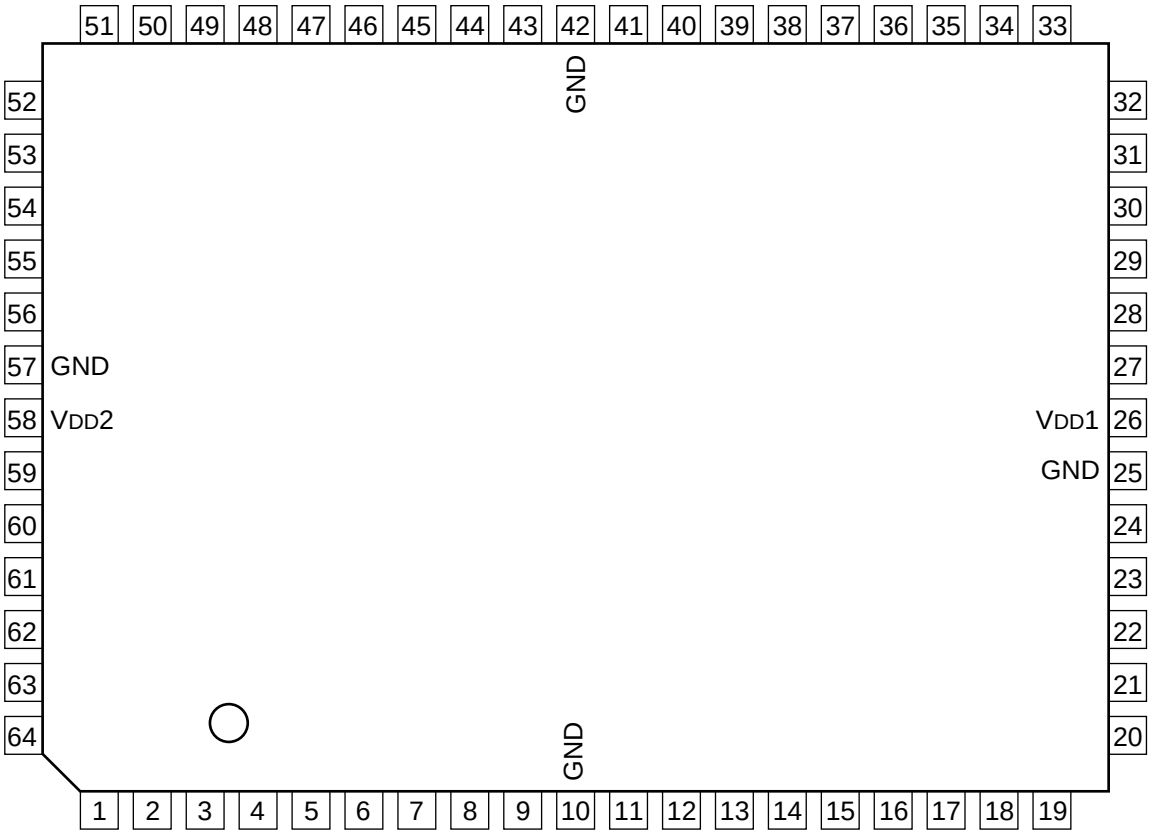
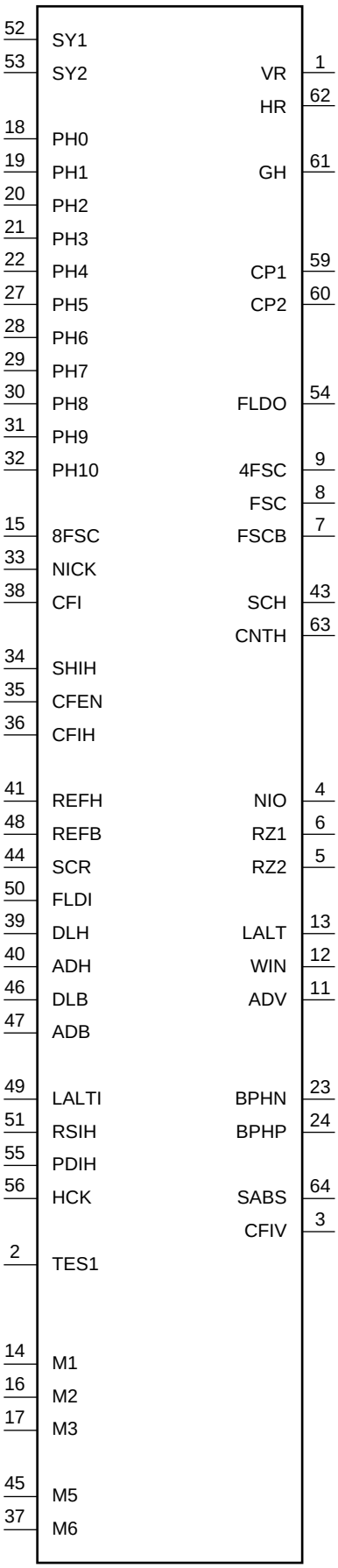
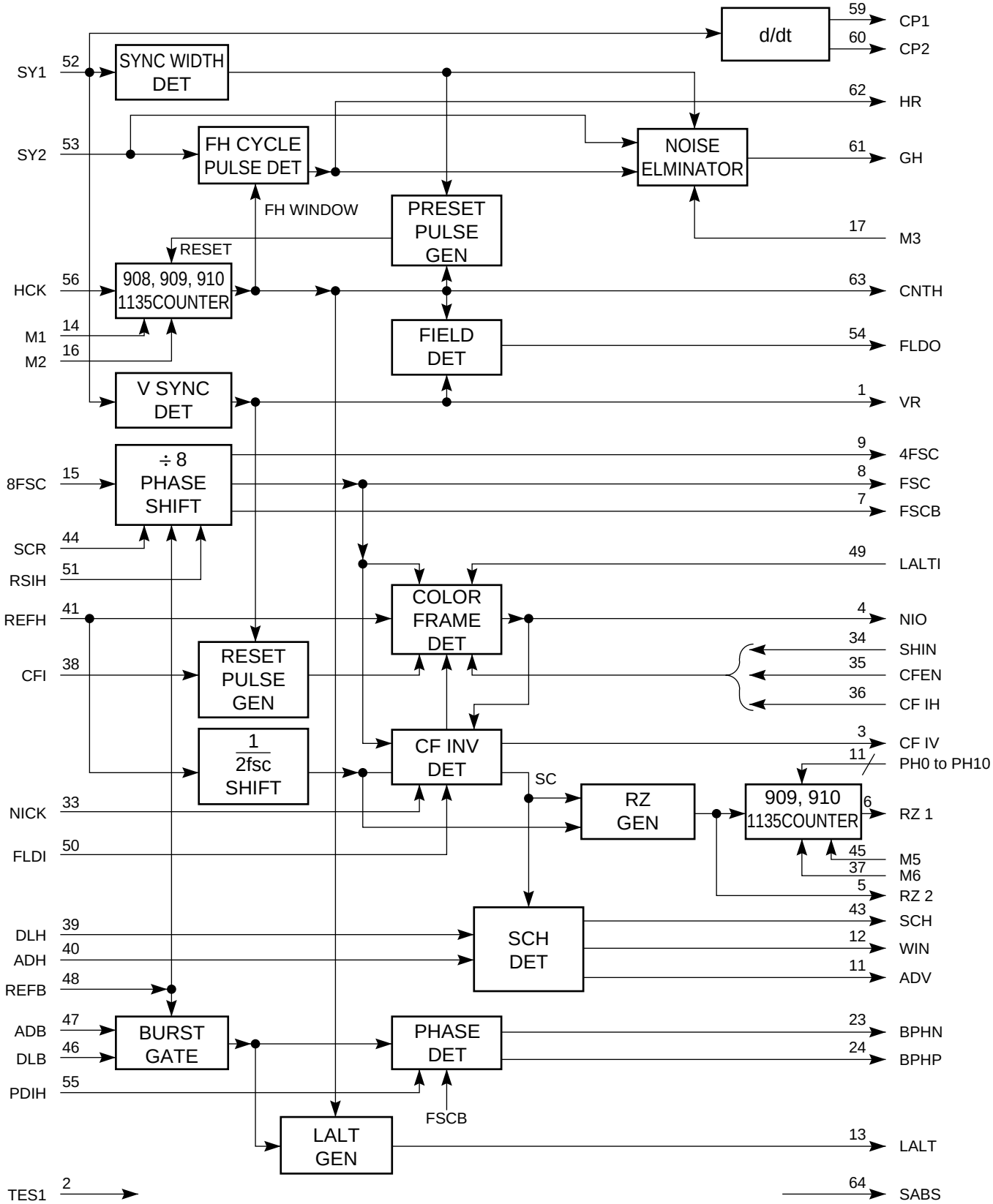
C-MOS VIDEO CLOCK GENERATOR

—TOP VIEW—



CXD1312Q(2/9)


52 SY1
53 SY2
18 PH0
19 PH1
20 PH2
21 PH3
22 PH4
27 PH5
28 PH6
29 PH7
30 PH8
31 PH9
32 PH10
15 8FSC
33 NICK
38 CFI
34 SHIH
35 CFEN
36 CFIH
41 REFH
48 REFB
44 SCR
50 FLDI
39 DLH
40 ADH
46 DLB
47 ADB
49 LALTI
51 RSIH
55 PDIH
56 HCK
2 TES1
14 M1
16 M2
17 M3
45 M5
37 M6
VR 1
HR 62
GH 61
CP1 59
CP2 60
FLDO 54
4FSC 9
FSC 8
FSCB 7
SCH 43
CNTH 63
NIO 4
RZ1 6
RZ2 5
LALT 13
WIN 12
ADV 11
BPHN 23
BPHP 24
SABS 64
CFIV 3


d/dt
59
CP1
60
CP2
SY1
52
SYNC WIDTH DET
62
HR
SY2
53
FH CYCLE PULSE DET
NOISE ELMINATOR
61
GH
FH WINDOW
PRESET PULSE GEN
17
M3
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56
908, 909, 910 1135COUNTER
63
CNTH
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14
M2
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FIELD DET
54
FLDO
V SYNC DET
1
VR
÷ 8 PHASE SHIFT
9
4FSC
8FSC
15
8
FSC
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FSCB
SCR
44
RSIH
51
49
LALTI
COLOR FRAME DET
REFH
41
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NIO
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SHIN
RESET PULSE GEN
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1/2fsc SHIFT
CF INV DET
3
CF IV
11
PH0 to PH10
SC
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909, 910 1135COUNTER
NICK
33
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RZ 1
FLDI
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M5
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M6
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RZ 2
43
SCH
DLH
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SCH DET
12
WIN
ADH
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ADV
REFB
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ADB
47
BURST GATE
PHASE DET
23
BPHN
DLB
46
24
BPHP
PDIH
55
FSCB
LALT GEN
13
LALT
TES1
2
64
SABS

PIN NO.	SIGNAL	DESCRIPTION

1. VR out — **V SYNC PULSE output**

VR is derived from the SY1(pin 52) input.

2. TES1 in — **TEST MODE input**

TES1	MODE
0	TEST
(1)	NORMAL

0 : Low level
(0) : Low level or open
1 : High level
(1) : High level or open

3. CFIV out — **TEST SIGNAL output**

4. NIO out — **1/2 NI CLOCK output**

The frequency of NIO is a half of the NICK(pin 33) input.

5. RZ2 out — **READ ZERO 2 output**

RZ2 is derived from the REFH (pin 41) input and shows the starting timing of each line.

6. RZ1 out — **READ ZERO 1 output**

RZ1 is derived from RZ2 (pin 5). RZ1 is delayed by PH0 to PH10 inputs. See the description of the PH0 (pin 18) input.

7. FSCB out — **FSCB PULSE output**

FSCB is derived from FSC (pin 8) and its phase is shifted by the LALT I(pin 49) input. The amount of shift is one clock length of the 4FSC (pin-9) input.

8. FSC out — **FSC CLOCK output**

9. 4FSC out — **4FSC CLOCK output**

These are derived from the 8FSC (pin 15) input.

10. GND — **GND**

11. ADV out — **SC-H ADVANCE output**

12. WIN out — **SC-H IN PHASE output**

These signals shows the SC-H phase. See the description of the DLH (pin 39) input.

13. LALT out — **PAL PULSE output**

The LALT output is derived from the REFB(pin 48) burst signal in the pal system.

14. M1 in **HCK FREQUENCY SELECT input**

Set M1 and M2 (pin 16) as follows according as the frequency of the HCK (pin 56) input.

FREQ. OF HCK	M1	M2
908 FH	0	0
910 FH	0	(1)
909 FH	(1)	0
1135 FH	(1)	(1)

FH : Frequency of the H sync signal that composes the SY2 (pin 53) input.

15. 8FSC in **8FSC CLOCK input**

The rising edge is active.
4FSC (pin 9) , FSC (pin 8) and FSCB (pin 7) are derived from 8FSC.

16. M2 in **HCK FREQUENCY SELECT input**

See the description of the M1 (pin 14) input.

17. M3 in **NOISE ELIMINATOR ON/OFF SELECT input**

M3 sets the noise eliminator for the GH (pin 61) output derived from the SY2 (pin 53) input on or off.

M3	NOISE ELIMINATION
0	OFF
(1)	ON

18. PH0 in **DELAY CONTROL INPUT FOR RZ1**
19. PH1 in **DELAY CONTROL INPUT FOR RZ1**
20. PH2 in **DELAY CONTROL INPUT FOR RZ1**
21. PH3 in **DELAY CONTROL INPUT FOR RZ1**
22. PH4 in **DELAY CONTROL INPUT FOR RZ1**

These inputs control the delay time of the RZ1 (pin 6) output as follows:

PH10 to PH0 INPUTS							DELAY TIME OF RZ1
10	9	8	— —	2	1	0	
0	0	0	— —	0	0	0	1/(4 Fsc) × 2047
0	0	0	— —	0	0	1	1/(4 Fsc) × 2046
0	0	0	— —	0	1	0	1/(4 Fsc) × 2045
0	0	0	— —	0	1	1	1/(4 Fsc) × 2044
1	1	1	— —	1	0	0	1/(4 Fsc) × 3
1	1	1	— —	1	0	1	1/(4 Fsc) × 2
1	1	1	— —	1	1	0	1/(4 Fsc) × 1
1	1	1	— —	1	1	1	1/(4 Fsc) × 0

23. BPHN out **BURST PHASE-N output**
24. BPHP out **BURST PHASE-P output**

These are the outputs of the phase comparator between the DLB (pin 46)/ADB (pin 47) inputs and the internal SC that is equivalent to the FSCB (pin 7) output.
The PDIH (pin 55) input inhibits the BPHN and BPHP outputs.

PDIH	BPHN/BPHP OUTPUTS
(0)	INHIBIT
1	ENABLE

25. GND **GND**
26. VDD1 **+5V input**

27. PH5 in **DELAY CONTROL INPUT FOR RZ1**
28. PH6 in **DELAY CONTROL INPUT FOR RZ1**
29. PH7 in **DELAY CONTROL INPUT FOR RZ1**
30. PH8 in **DELAY CONTROL INPUT FOR RZ1**
31. PH9 in **DELAY CONTROL INPUT FOR RZ1**
32. PH10 in **DELAY CONTROL INPUT FOR RZ1**

These inputs control the delay time of the RZ1 (pin 6) output. See the description of PH0(pin 18) input.

33. NICK in **NI CLOCK input**

NICK is the clock pulse to generate the NI (normal/invert) pulse to be used internally. Usually, CNTH (pin 63) for the NTSC system or LALT (pin 13) for the PAL system is input to this terminal.
The rising edge is active.

34. SHIH in **MODE SELECT (COLOR FRAMING DET./RZ GEN) input**
35. CFEN in **MODE SELECT (COLOR FRAMING DET./RZ GEN) input**
36. CFIH in **MODE SELECT (COLOR FRAMING DET./RZ GEN) input**

These inputs set CXD1312Q to the color framing detector mode or the read zero generator mode as follows:

SHIH	CFEN	CFIH	MODE
0	(0)	1	COLOR FRAMING DETECTOR
(1)	(0)	(0)	RZ GENERATOR

37. M6 in **SIGNAL SYSTEM SELECT input**

Set M5 (pin 45) and M6 as follows according as the video signal to be used.

MODE & VIDEO SIGNAL	M5	M6
TEST	0	0
4FSC/FH=909 : PALM	0	(1)
4FSC/FH=910 : NTSC	(1)	0
4FSC/FH=1135: PAL	(1)	(1)

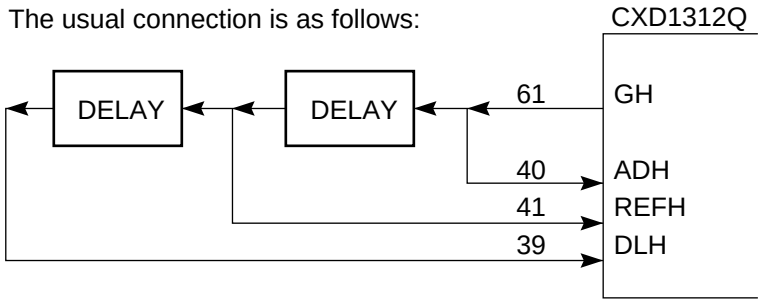
38. CFI in **COLOR FRAME PULSE input**

This pulse is used for resetting the internal LALT signal in the RZ GENERATOR mode.

39. DLH in **DELAY H input**

40. ADH in **ADVANCE H input**

These H signals are used for the SC-H phase detection. The SC-H phase detector outputs ADV (pin 11) and WIN (pin 12) according as the phase relation between DLH/ADH and the internal SC that is equivalent to FSC (pin 8).
If the internal SC is between ADH and DLH, the WIN output goes to LOW.
If the internal SC is in advance of ADH, the ADV output goes to LOW.
The usual connection is as follows:



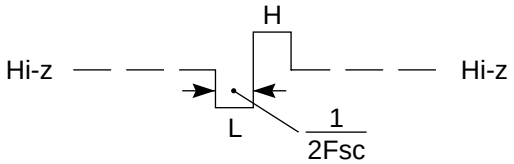
41. REFH in **REFERENCE H PULSE input**

REFH is used for the color framing detector and the RZ generator. GH (pin 61) or HR (pin 62) is usually input to this terminal.

42. GND **GND**

43. SCH out **SC-H PHASE output**

This signal shows the phase difference between REFH (pin 41) and internal SC. When they are in phase, the SCH output is as folows:



44. SCR in **DIRECT RESET INPUT FOR DIVIDE-BY-8 COUNTER**

This signal resets the divide-by-8 counter of 8FSC (pin 15) input directly.

SCR	DIVIDE-BY-8 COUNTER
(0)	RESET
1	COUNT

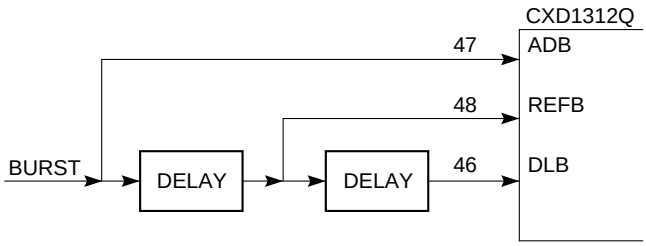
45. M5 in **SIGNAL SYSTEM SELECT input**

See the description of the M6 (pin 37) input.

46. DLB in **DELAY BURST input**

47. ADB in **ADVANCE BURST input**

These burst signals are used for phase comparison with the internal SC.
The usual connection is as follows:



48. REFB in **REFERENCE BURST input**

REFB is used for resetting the divide-by-8 counter. RSIH (pin 51) inhibits the resetting as follows:

RSIH	RESET BY BY REFB
(0)	INHIBIT
1	ENABLE

49. LALTI in **PAL PULSE input**

The PAL pulse should be input to this terminal for the PAL system, but this terminal should be kept open for the NTSC system.

50. FLDI in **PAL FIELD PULSE input**

Phase alternating pulse by field.
The FLDO (pin 54) output is usually input to this terminal for the PAL system, but this terminal should be kept open for the NTSC system.

51. RSIH in **RESET INHIBIT input**

This signal inhibits for the REFB (pin 48) input to reset the divide-by-8 counter of 8FSC (pin 15) input.
See the description of the REFB (pin 48) input.

52. SY1 in **ROUGH SYNC PULSE input (negative pulse)**

VR (pin 1) , CP1 (pin 59) , CP2 (pin 60) and the internal gate pulse are derived from SY1.

53. SY2 in **SYNC PULSE input (negative pulse)**

This sync pulse generates GH (pin 61) , and GH is input to the SC-H phase detection circuit. See the description of DLH (pin 39) and ADH (pin 40).

54. FLDO out **FIELD PULSE output**

Phase altering pulse by field.

55. PDIH in **BPHN/BPHP OUTPUT INHIBIT input**

This signal inhibits the BPHN (pin 23) and BPHP (pin 24) outputs. See the description of BPHN and BPHP.

56. HCK in **nH CLOCK input**

The frequency of the HCK input has the specified relation with that of the H sync signal that composes the SY2 (pin 53) input. See the description of the M1 (pin 14) input.

57. GND **GND**

58. VDD2 **+5 V input**

59. CP1 out **LEADING EDGE OF SY1 (pin 52) output**

60. CP2 out **TRAILING EDGE OF SY1 (pin 52) output**

61. GH out **GATED H PULSE output**

62. HR out **H PULSE output**

GH and HR are derived from the SY2 (pin 53) sync pulse input. Both signals consist of H pulses but not of a half H pulse.
GH is processed by the noise eliminator and loses nine pulses in the V sync interval.

63. CNTH out **COUNT H output**

CNTH is a H pulse signal that is divided from the HCK (pin 56) input . the divider is reset by the SY1 (pin 52) input.
See the description of the M1 (pin 14) input.

64. SABS out **TEST output**