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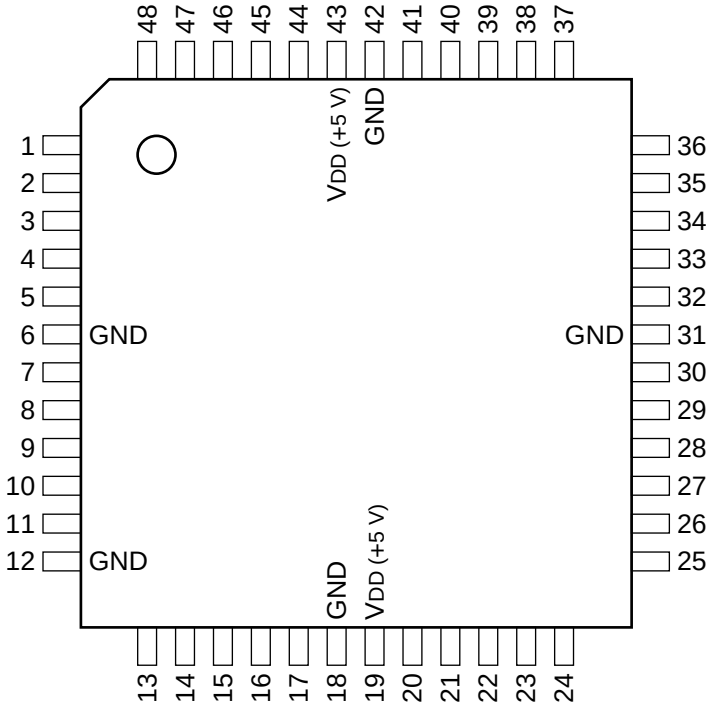
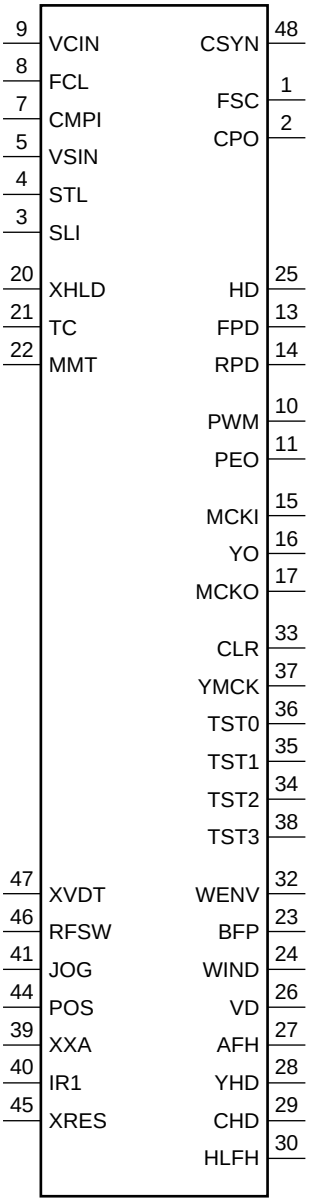
C-MOS AUTOMATIC FREQUENCY CONTROL (AFC)/SYNC SEPARATOR

—TOP VIEW—



(V_{DD} = +5 V)

PIN NO.	I/O	SYMBOL	PIN NO.	I/O	SYMBOL	PIN NO.	I/O	SYMBOL	PIN NO.	I/O	SYMBOL
1	I/O	FCS	13	O	FPD	25	O	HD	37	I	YMCK
2	I/O	CPO	14	O	RPD	26	O	VD	38	O	TST3
3	I	SLI	15	I	MCKI	27	O	AFH	39	I/O	XXA
4	I	STL	16	O	YO	28	O	YHD	40	I/O	IR1
5	I	VSIN	17	O	MCKO	29	O	CHD	41	I	JOG
6	—	GND	18	—	GND	30	O	HLFH	42	—	GND
7	I	CMPI	19	—	V_{DD}	31	—	GND	43	—	V_{DD}
8	I	FCL	20	I	XHLD	32	O	WEVN	44	I	POS
9	I	VCIN	21	O	TC	33	I	CLR	45	O	XRES
10	I	PWM	22	I	MMT	34	I	TST2	46	I	RFSW
11	O	PEO	23	O	BFP	35	I	TST1	47	I	XVDT
12	—	GND	24	O	WIND	36	I	TST0	48	O	CSYN



INPUT

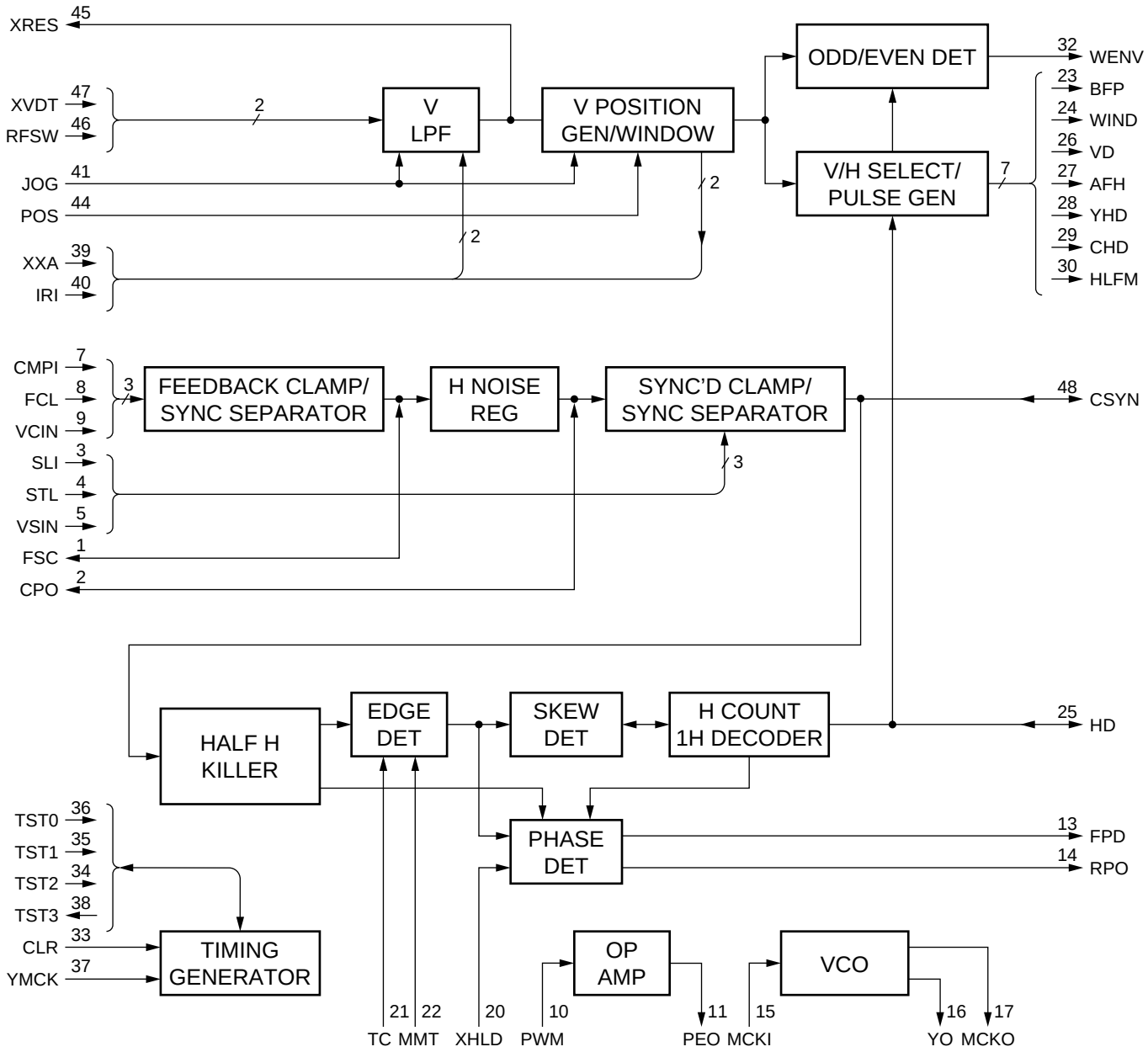
CLR	;	DIRECT CLEAR
CMPI	;	FEEDBACK CLAMP SLICE LEVEL
FCL	;	FEEDBACK CLAMP SYNC CHIP LEVEL
JOG	;	REFERENCE CONTROL
MCKI	;	CLOCK (VCO) INVERTER
MMT	;	MONOSTABLE MULTIVIBRATOR TEST PIN (H : NORMAL)
POS	;	PHASE REFERENCE SELECT
PWM	;	OPERATIONAL AMPLIFIER
RFSW	;	RF SWITCHING PULSE
SLI	;	SYNC CLAMP SLICE LEVEL
STL	;	SYNC CLAMP SYNC CHIP LEVEL
TST0	;	L : NORMAL/H : TEST MODE
TST1, TST2	;	AFC LOCK PHASE COARSE ADJUST
VCIN	;	FEEDBACK CLAMP VIDEO
VSIN	;	SYNC CLAMP VIDEO
XHLD	;	H : AFC ERROR ACTIVE/L : AFC ERROR HOLD
XVDT	;	V DETECT COMPOSITE SYNC
YMCK	;	MASTER CLOCK

OUTPUT

AFH	;	AFC H DRIVE
BFP	;	BURST FLAG PULSE
CHD	;	H SYNC OUTPUT FOR BURST DETECT
FPD	;	AFC SUB LOOP PHASE ERROR
HLFH	;	1/2 f_H (≒7.5 kHz)
MCKO	;	CLOCK (VCO) INVERTER (910 f_H)
PEO	;	OPERATIONAL AMPLIFIER
RPD	;	AFC MAIN LOOP PHASE ERROR
TST3	;	L : NORMAL, H : TEST MODE
VD	;	VERTICAL SYNC DETECT
WEVN	;	WRITE EVEN/ODD FIELD DETECT
WIND	;	WINDOW COMPARATOR OUTPUT FOR V-PLL
XRES	;	V DETECT LPF
YO	;	CLOCK (VCO) INVERT
YHD	;	PEDESTAL CLAMP TIMING

INPUT/OUTPUT

CPO	;	CLAMP PULSE
CSYN	;	CLAMP SYNC SEPARATE
FCS	;	FEEDBACK CLAMP SYNC SEPARATE
HD	;	AFC H DIRECT
IR1	;	MONITOR PIN FOR TEST
TC	;	AFC LOCK PHASE FINE ADJUST
XXA	;	MONITOR PIN FOR TEST


XRES
45
XVDT
47
RFSW
46
2
V
LPF
V POSITION
GEN/WINDOW
ODD/EVEN DET
32
WENV
23
BFP
24
WIND
26
VD
27
AFH
28
YHD
29
CHD
30
HLFM
V/H SELECT/
PULSE GEN
7
JOG
41
POS
44
2
2
XXA
39
IRI
40
CMPI
7
FCL
8
VCIN
9
3
FEEDBACK CLAMP/
SYNC SEPARATOR
H NOISE
REG
SYNC'D CLAMP/
SYNC SEPARATOR
48
CSYN
SLI
3
STL
4
VSIN
5
3
FSC
1
CPO
2
HALF H
KILLER
EDGE
DET
SKEW
DET
H COUNT
1H DECODER
25
HD
TST0
36
TST1
35
TST2
34
TST3
38
PHASE
DET
13
FPD
14
RPO
CLR
33
YMCK
37
TIMING
GENERATOR
OP
AMP
VCO
21
22
20
10
11
15
16
17
TC
MMT
XHLD
PWM
PEO
MCKI
YO
MCKO