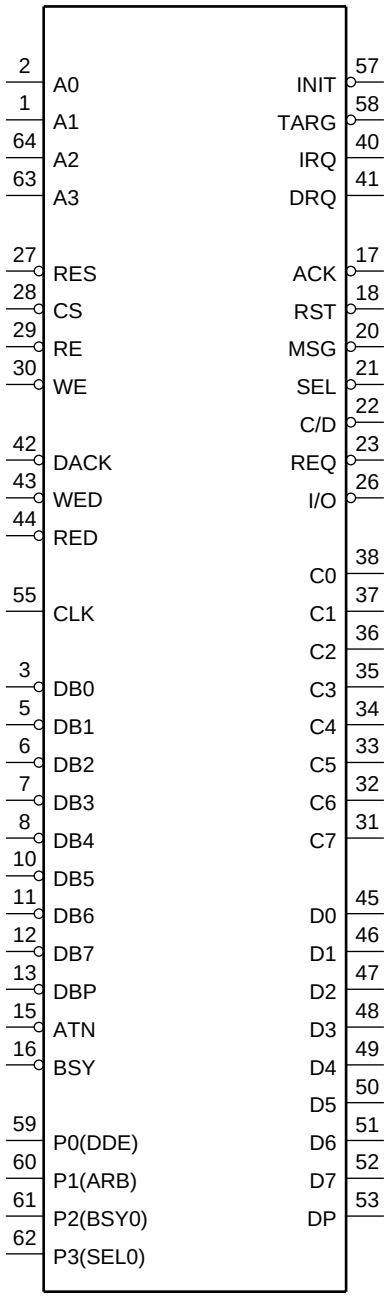

INPUT

A0-A3	; REGISTER SELECT
$\overline{CS}$	; CHIP SELECT
$\overline{RES}$	; RESET
$\overline{RE}$	; READ ENABLE
$\overline{WE}$	; WRITE ENABLE
$\overline{DACK}$	; ACKNOWLEDGE FOR DMA REQUEST
$\overline{WED}$	; WRITE ENABLE (DATA BUS)
$\overline{RED}$	; READ ENABLE (DATA BUS)
$\overline{CLK}$	; CLOCK

OUTPUT

IRQ	; INTERRUPTION REQUEST
DRQ	; DMA REQUEST
$\overline{INIT}$	; INITIATOR SELECT
$\overline{TARG}$	; TARGET SELECT

INPUT/OUTPUT

$\overline{DB0}$-$\overline{DB7}$	; DATA BUS
$\overline{DBP}$	; DATA BUS UNEVEN PARITY
$\overline{ATN}$	; ATTENUATOR (SCSI BUS)
$\overline{BSY}$	; BUSY (SCSI BUS)
$\overline{ACK}$	; ACKNOWLEDGE (SCSI BUS)
$\overline{RST}$	; RESET (SCSI BUS)
$\overline{MSG}$	; MESSAGE (SCSI BUS)
$\overline{SEL}$	; SELECT (SCSI BUS)
$\overline{C/D}$	; C/D SIGNAL (SCSI BUS)
$\overline{REQ}$	; REQUEST (SCSI BUS)
$\overline{I/O}$	; INPUT/OUTPUT SIGNAL (SCSI BUS)
C0-C7	; CPU BUS
D0-D7	; DATA BUS
DP	; DATA BUS PARITY
P0-P3	; PORT