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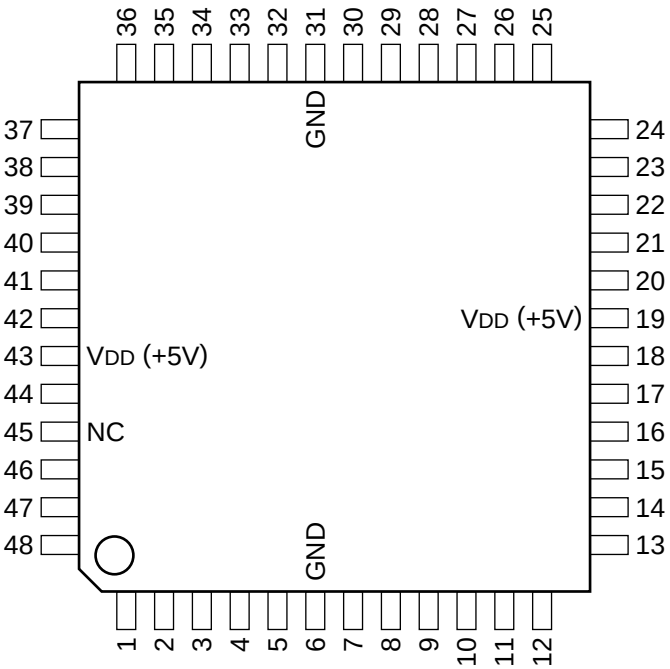
IL08

C-MOS PCM AUDIO SELECTOR FOR CADA SYSTEM

-TOP VIEW-



(VDD = +5V)

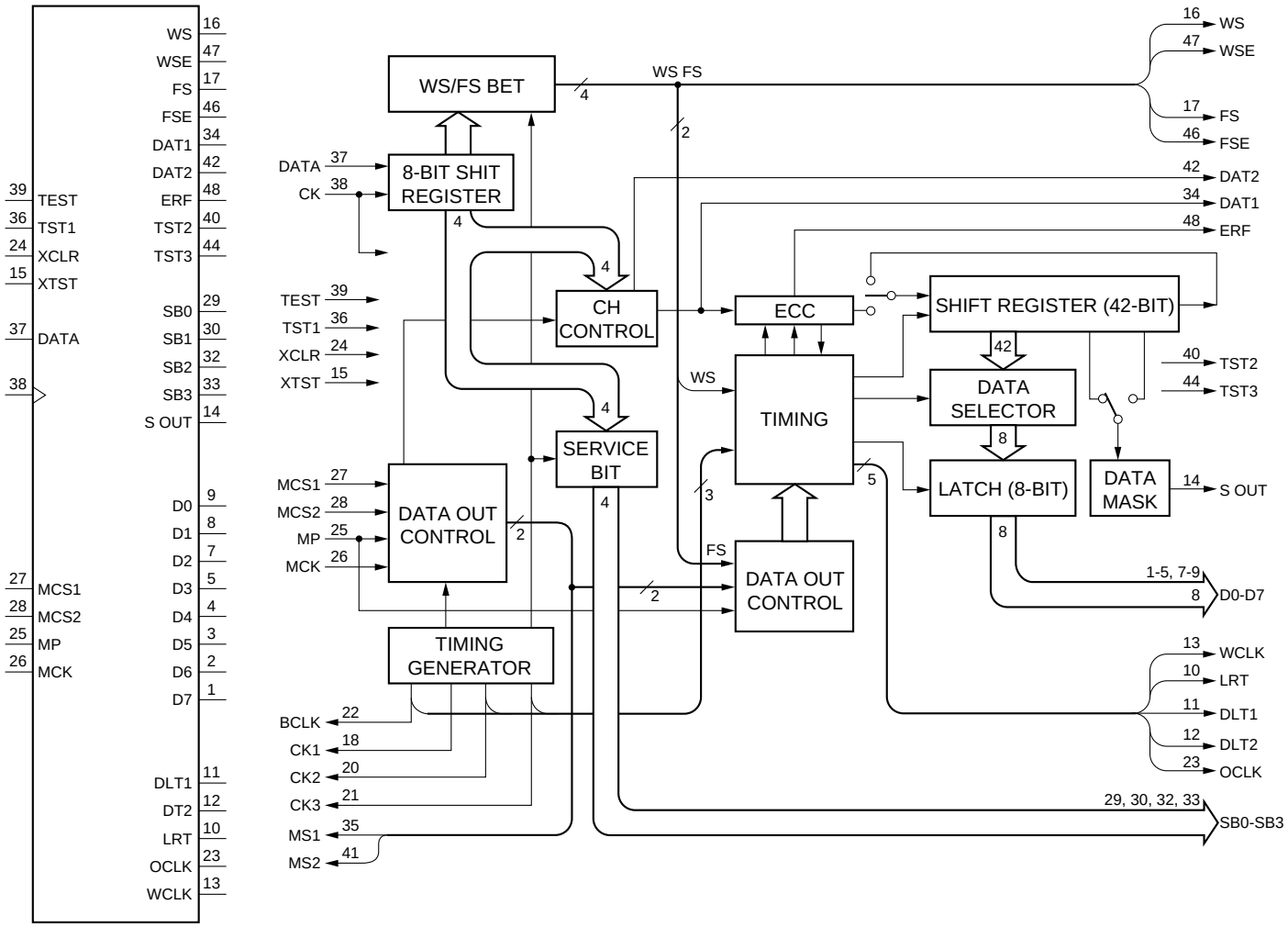
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	D7	13	O	WCLK	25	I	MP	37	I	DATA
2	O	D6	14	O	SOUT	26	I	MCK	38	I	CK
3	O	D5	15	I	XTST	27	I	MCS1	39	I	TEST
4	O	D4	16	O	WS	28	I	MCK2	40	O	TST2
5	O	D3	17	O	FS	29	O	SB0	41	O	MS2
6	—	GND	18	O	CK1	30	O	SB1	42	O	DAT2
7	O	D2	19	—	VDD	31	—	GND	43	—	VDD
8	O	D1	20	O	CK2	32	O	SB2	44	O	TST3
9	O	D0	21	O	CK3	33	O	SB3	45	—	NC
10	O	LRT	22	O	BCLK	34	O	DAT1	46	O	FSE
11	O	DLT1	23	O	OCLK	35	O	MS1	47	O	WSE
12	O	DLT2	24	I	XCLR	36	I	TST1	48	O	ERF

INPUT

CK	; MASTER CLOCK (7.4 MHz)
DATA	; INPUT DATA
MCK	; SERIAL DATA TRANSMISSION CLOCK FOR MODE SETTING
MCS1, MCS2	; CONTROL (1-2) FOR MODE SETTING
MP	; SERIAL DATA FOR MODE SETTING
TEST	; TEST (NORMALLY LOW LEVEL)
TST1	; TEST (NORMALLY LOW LEVEL)
XCLR	; INTERNAL INTIAL SETTING (NORMALLY HIGH LEVEL)
XTST	; TEST (NORMALLY HIGH LEVEL)

OUTPUT

BCLK	; CLOCK (1.85 MHz)
CK1	; CLOCK (88.2 MHz)
CK2	; CLOCK (44.1 MHz)
CK3	; CLOCK (22.05 MHz)
D0-D7	; PARALLEL DATA (0-7)
DAT1, DAT2	; OUTPUT DATA (1-2)
DLT1, DLT2	; DAC TIMING SIGNAL (1-2)
ERF	; ERROR FLAG
FS	; FRAME SYNC
FSE	; FRAME SYNC ERROR
LRT	; L/R CHANNEL SERECT SIGNAL
MS1, MS2	; MODE SET (1-2)
OCLK	; CLOCK (1.85 MHz)
SB0-SB3	; SERVICE BIT (0-3)
SOUT	; SERIAL DATA OUTPUT
TST2, TST3	; TEST (2-3)
WCLK	; WORD CLOCK
WS	; WORD SYNC
WSE	; WORD SYNC ERROR


WS
WSE
FS
FSE
DAT1
DAT2
ERF
TST2
TST3
SB0
SB1
SB2
SB3
S OUT
D0
D1
D2
D3
D4
D5
D6
D7
DLT1
DT2
LRT
OCLK
WCLK
TEST
TST1
XCLR
XTST
DATA
MCS1
MCS2
MP
MCK
WS/FS BET
WS FS
8-BIT SHIT REGISTER
CH CONTROL
SERVICE BIT
DATA OUT CONTROL
TIMING GENERATOR
ECC
TIMING
SHIFT REGISTER (42-BIT)
DATA SELECTOR
LATCH (8-BIT)
DATA MASK
DATA OUT CONTROL
BCLK
CK1
CK2
CK3
MS1
MS2
1-5, 7-9
D0-D7
29, 30, 32, 33
SB0-SB3