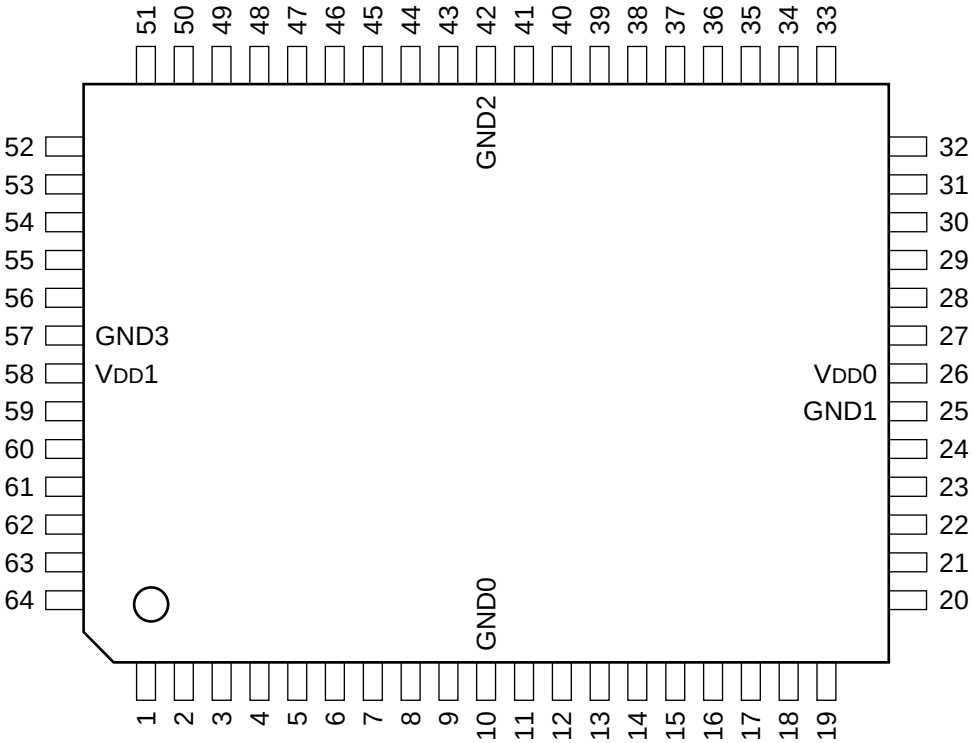
C-MOS DIGITAL AFM EXPANDER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	DTVI	17	O	PBVO	33	O	FM14	49	I	D22
2	I	RS0I	18	I	AS0I	34	O	FM13	50	I	D23
3	I	RS1I	19	I	AS1I	35	O	FM12	51	O	RZ2O
4	O	CHO	20	O	ASWO	36	O	FM11	52	I	D10
5	I	CSHI	21	O	SW1O	37	O	FM10	53	I	D11
6	I	CGBI	22	O	SW2O	38	O	FM27	54	I	D12
7	I	MD0I	23	I	ROEI	39	O	FM26	55	I	D13
8	I	MD1I	24	I	R27I	40	O	FM25	56	O	RZ1O
9	I	W2CKI	25	—	GND1	41	O	FM24	57	—	GND3
10	—	GND0	26	—	VDD0	42	—	GND2	58	—	VDD1
11	O	WCKO	27	O	R9O	43	O	FM23	59	O	WZO
12	I	VTMI	28	I	R2CKI	44	O	FM22	60	O	CTVO
13	I	YSI	29	O	RCKO	45	O	FM21	61	O	S2HO
14	I	YDOI	30	O	FM17	46	O	FM20	62	I	TM0I
15	O	TVP	31	O	FM16	47	I	D20	63	I	TM1I
16	O	TTM	32	O	FM15	48	I	D21	64	I	CLRI

INPUT

AS0I, AS1I	:	SET PIN FOR CHANGING SWITCHING POSITION OF AUDIO SWITCHING PULSE ASWO
CGBI	:	GUARD BAND INFORMATION DETECTED BY TBC (L : CHO IS RESET BY CSHI)
CLRI	:	MASTER CLEAR (L : CLEAR)
CSHI	:	C-SH INPUT CREATED FROM PLAYED BACK C-SYNC BY DISCRIMINATING ITS PERIOD BY TBC
DTVI	:	EXTERNAL DTV INPUT NORMALLY, LOADED BY PBV.
D10 - D13	:	MEMORY READ FIRST PORT OUT (RF A CHANNEL)
D20 - D23	:	MEMORY READ SECOND PORT OUT (RF B CHANNEL)
MD0I, MD1I	:	MODE
ROEI	:	REFERENCE ODD/EVEN INPUT (L : 1st FIELD)
RS0I, RS1I	:	DETERMINES RESET TIMING OF CHO BY CSH (CSHI)
R2CKI	:	TWICE READ CLOCK
R27I	:	REFERENCE 27 MHz CLOCK
TM0I, TM1I	:	TEST MODE SET PIN
VTMI	:	SET PIN FOR PROVIDING TIME LIMITATION AT DETECTION POINT OF DETECTING INTEGRATION COUNTER DURING V SYNC SEP (H : TIMER ON)
W2CKI	:	TWICE WRITE CLOCK CREATED BY PLL (PAL = 576 fh, NTSC = 572 fh)
YDOI	:	DO PULSE INPUT OF PLAYBACK Y-RF (L : DO)
YSI	:	PB-Y SYNC

OUTPUT

ASWO	:	SWITCHING PULSE SWITCHING POSITION IS SET BY AS0I AND AS1I. (L : 1st FIELD = AcH)
CHO	:	COUNTER H OUTPUT FOR GENERATING CLOCK SYNCHRONIZED WITH PLAYBACK C-SYNC
CTVO	:	V COUNTER CARRY OUT
FM10 - FM17	:	D1 SIDE (RF A cH) DATA IT IS OUTPUT WHEN SW1O IS HIGH. (1st FIELD)
FM20 - FM27	:	D2 SIDE DATA IT IS OUTPUT WHEN SW2O IS LOW. (2nd FIELD)
PBVO	:	V DETECTED PB-V PULSE
RCKO	:	1/2 DIVIDED READ CLOCK OF R2CKI
RZ1O	:	READ ZERO FOR MEMORY FIRST PORT, CREATED FROM ROEI FALLING EDGE
RZ2O	:	READ ZERO FOR MEMORY SECOND PORT, CREATED FROM ROEI RISING EDGE
R9O	:	1/3 DIVIDED OUTPUT OF 27 MHz CLOCK OF R27I
SW1O	:	SWITCHING PULSE FOR OVER-LAP SWITCHING FOR TEST
SW2O	:	REVERSED DUTY SWITCHING PULSE TO SWITCHING PULSE OF SW1O FOR TEST
S2HO	:	1/2 H SELF-PROPELLED 2 fh COUNTER
TTM	:	TEST GATE PULSE FOR DETECTING V IS NORMAL OUTPUT.
TVP	:	TEST 1CK LATCHED NEGATIVE PULSE IS OUTPUT.
WCKO	:	1/2 DIVIDED CLOCK OUTPUT OF W2CKI
WZO	:	MEMORY WRITE ZERO