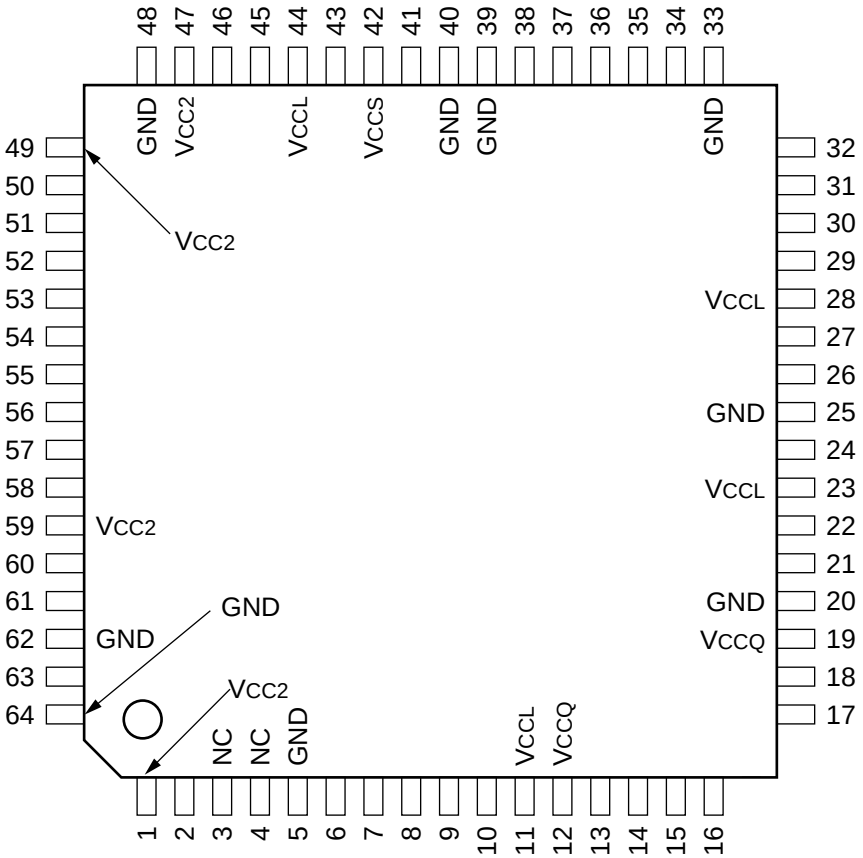
SERIAL DIGITAL INTERFACE TRANSMISSION DECODER

—TOP VIEW—



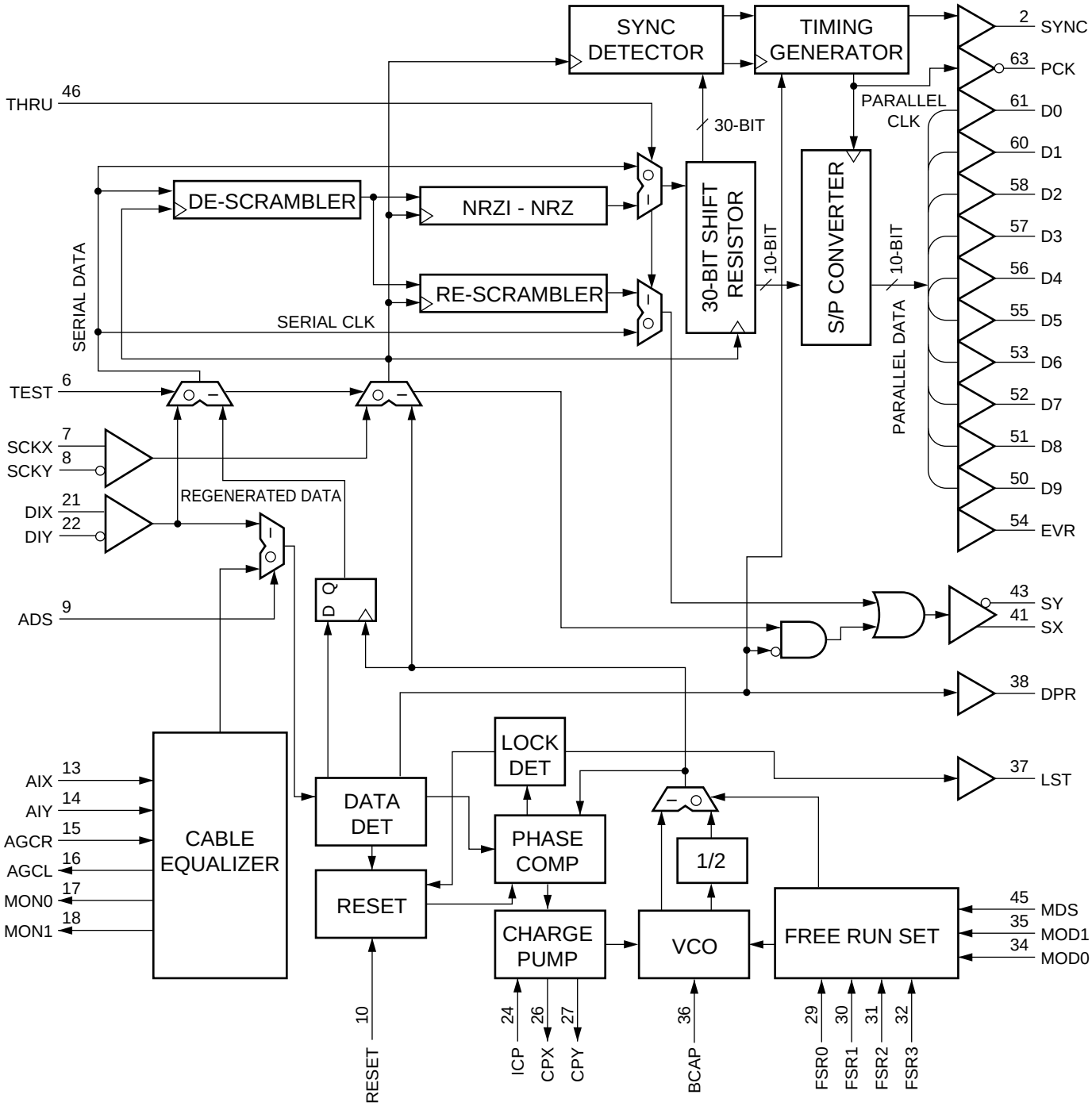
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V_{CC2}	17	O	MON0	33	—	GND	49	—	V_{CC2}
2	O	SYNC	18	O	MON1	34	I	MOD0	50	O	D9
3	—	NC	19	—	V_{CCQ}	35	I	MOD1	51	O	D8
4	—	NC	20	—	GND	36	I	BCAP	52	O	D7
5	—	GND	21	I	DIX	37	O	LST	53	O	D6
6	I	TEST	22	I	DIY	38	O	DPR	54	O	EVR
7	I	SCKX	23	—	V_{CCL}	39	—	GND	55	O	D5
8	I	SCKY	24	I	ICP	40	—	GND	56	O	D4
9	I	ADS	25	—	GND	41	O	SX	57	O	D3
10	I	RESET	26	O	CPX	42	—	V_{CCS}	58	O	D2
11	—	V_{CCL}	27	O	CPY	43	O	SY	59	—	V_{CC2}
12	—	V_{CCQ}	28	—	V_{CCL}	44	—	V_{CCL}	60	O	D1
13	I	AIX	29	I	FSR0	45	I	MDS	61	O	D0
14	I	AIY	30	I	FSR1	46	I	THRU	62	—	GND
15	I	AGCR	31	I	FSR2	47	—	V_{CC2}	63	O	PCK
16	O	AGCL	32	I	FSR3	48	—	GND	64	—	GND

INPUT

ADS	:	TEST
AGCR	:	AGC REFERENCE VOLTAGE
AIX, AIY	:	SERIAL DATA
BCAP	:	EXTERNAL CAPACITOR FOR VCO
DIX, DIY	:	TEST
FSR0 - FSR3	:	EXTERNAL RESISTOR FOR SETTING THE VCO FREE-RUN FREQUENCY
ICP	:	CHARGE PUMP CURRENT SETTING
MDS	:	TEST
MOD0, MOD1	:	VCO RATE SELECT
RESET	:	PLL RESET
SCKX, SCKY	:	TEST
TEST	:	TEST
THRU	:	TEST

OUTPUT

AGCL	:	EXTERNAL CAPACITOR FOR PEAK DETECTION
CPX, CPY	:	CHARGE PUMP
D0 - D9	:	PARALLEL CLOCK
DPR	:	PLL LOCK STATUS
EVR	:	PARALLEL CLOCK
LST	:	PLL LOCK STATUS
MON0, MON1	:	EQUALIZER MONITOR
PCK	:	PARALLEL CLOCK
SX, SY	:	EXTERNAL RESISTOR FOR SERIAL DIFFERENTIAL OUTPUT
SYNC	:	PLL LOCK STATUS


SYNC DETECTOR
TIMING GENERATOR
2 SYNC
63 PCK
61 D0
60 D1
58 D2
57 D3
56 D4
55 D5
53 D6
52 D7
51 D8
50 D9
54 EVR
PARALLEL CLK
30-BIT
10-BIT
S/P CONVERTER
PARALLEL DATA
46 THRU
DE-SCRAMBLER
NRZI - NRZ
RE-SCRAMBLER
30-BIT SHIFT RESISTOR
SERIAL DATA
SERIAL CLK
6 TEST
7 SCKX
8 SCKY
21 DIX
22 DIY
REGENERATED DATA
9 ADS
D Q
43 SY
41 SX
38 DPR
LOCK DET
37 LST
13 AIX
14 AIY
15 AGCR
16 AGCL
17 MON0
18 MON1
CABLE EQUALIZER
DATA DET
RESET
PHASE COMP
1/2
CHARGE PUMP
VCO
FREE RUN SET
45 MDS
35 MOD1
34 MOD0
10 RESET
24 ICP
26 CPX
27 CPY
36 BCAP
29 FSR0
30 FSR1
31 FSR2
32 FSR3