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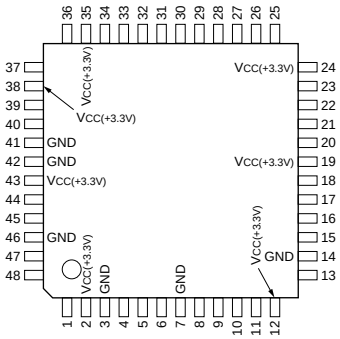
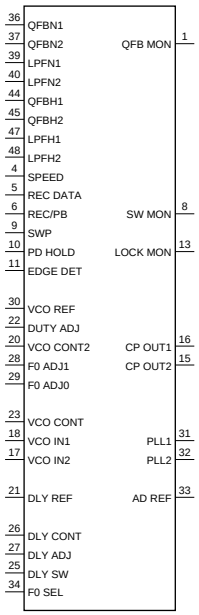
PHASE-LOCKED LOOP

– TOP VIEW–





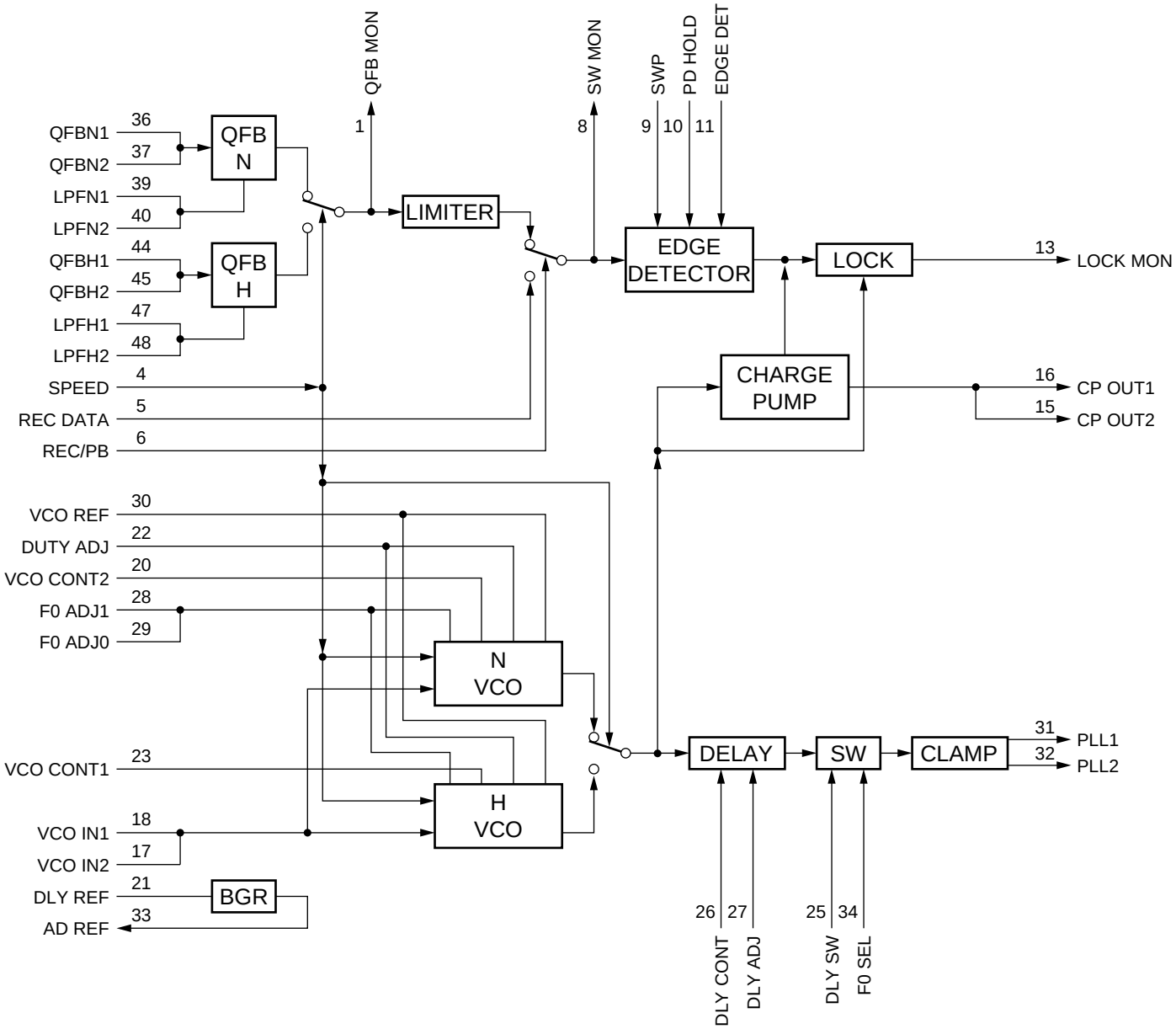
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	QFB MON	25	I	DLY SW
2	—	Vcc(+3.3V)	26	I	DLY CONT
3	—	GND	27	I	DLY ADJ
4	I	SPEED	28	I	F0 ADJ1
5	I	REC DATA	29	I	F0 ADJ0
6	I	REC/PB	30	I	VCO REF
7	—	GND	31	O	PLL1
8	O	SW MON	32	O	PLL2
9	I	SWP	33	O	AD REF
10	I	PD HOLD	34	I	F0 SEL
11	I	EDGE DET	35	—	Vcc(+3.3V)
12	—	Vcc(+3.3V)	36	I	QFBN1
13	O	LOCK MON	37	I	QFBN2
14	—	GND	38	—	Vcc(+3.3V)
15	O	CP OUT2	39	I	LPFN1
16	O	CP OUT1	40	I	LPFN2
17	I	VCO IN2	41	—	GND
18	I	VCO IN1	42	—	GND
19	—	Vcc(+3.3V)	43	—	Vcc(+3.3V)
20	I	VCO CONT2	44	I	QFBH1
21	I	DLY REF	45	I	QFBH2
22	I	DUTY ADJ	46	—	GND
23	I	VCO CONT1	47	I	LPFH1
24	—	Vcc(+3.3V)	48	I	LPFH2

INPUT

DLY ADJ	;	DELAY ADJUSTMENT
DLY CONT	;	DELAY CONTROL
DLY REF	;	EXTERNAL REFERENCE CURRENT SOURCE
DLY SW	;	OUTPUT POLARITY CONTROL (H : INVERT, L : NORMAL)
DUTY ADJ	;	VCO DUTY ADJUST
EDGE DET	;	EDGE PULSE WIDTH CONTROL
F0 ADJ1, F0 ADJ0	;	FREE-RUN FREQUENCY ADJUSTMENT
F0 SEL	;	FREE-RUN FREQUENCY SELECT
LPFH1, LPFH2	;	LOW-PASS FILTER FOR THE QFB
LPFN1, LPFN2	;	LOW-PASS FILTER FOR THE QFB
PD HOLD	;	HOLD MODE SELECT (H : HOLD, L : NORMAL)
QFBH1, QFBH2	;	PLAYBACK DATA INPUT
QFBN1, QFBN2	;	PLAYBACK DATA INPUT
REC DATA	;	RECORDING DATA
REC/PB	;	REC/PB SELECTOR (H : REC, L : PB)
SPEED	;	PLL SPEED SELECT
SWP	;	SWITCHING PULSE
VCO CONT1, VCO CONT2	;	VCO CENTER FREQUENCY CONTROL
VCO IN1, VCO IN2	;	DIFFERENTIAL ERROR INPUT
VCO REF	;	EXTERNAL REFERENCE CURRENT SOURCE

OUTPUT

AD REF	;	AD CONVERTER REFERENCE
CP OUT2, CP OUT1	;	COMPARATOR OUTPUT
LOCK MON	;	LOCK MONITOR
PLL1, PLL2	;	PLL OUTPUT
QFB MON	;	QUANTIZED FEEDBACK EQUALIZER MONITOR
SW MON	;	SW MONITOR


QFB MON
SW MON
SWP
PD HOLD
EDGE DET
1
8
9
10
11
QFBN1
QFBN2
LPFN1
LPFN2
QFBH1
QFBH2
LPFH1
LPFH2
36
37
39
40
44
45
47
48
QFB N
QFB H
LIMITER
EDGE DETECTOR
LOCK
13
LOCK MON
SPEED
REC DATA
REC/PB
4
5
6
CHARGE PUMP
16
15
CP OUT1
CP OUT2
VCO REF
DUTY ADJ
VCO CONT2
F0 ADJ1
F0 ADJ0
30
22
20
28
29
N VCO
VCO CONT1
23
H VCO
VCO IN1
VCO IN2
18
17
DLY REF
AD REF
21
33
BGR
DELAY
SW
CLAMP
31
32
PLL1
PLL2
26
27
25
34
DLY CONT
DLY ADJ
DLY SW
F0 SEL