SONY

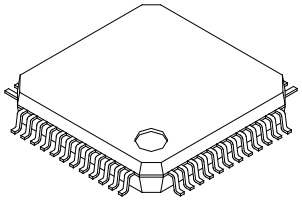
CXA1866Q

6-bit 140MSPS Flash A/D Converter

Description

The CXA1866Q is a 6-bit ultra-high-speed flash A/D converter IC capable of digitizing analog signals at the maximum rate of 140MSPS. The digital input level is compatible with ECL 100K/10KH/10K.

48 pin QFP (Plastic)



Features

- Ultra-high-speed operation with maximum conversion rate of 140MSPS
- Low input capacitance: 7pF
- Wide analog input bandwidth: 210MHz
- Low power consumption: 325mW
- Low error rate
- Excellent temperature characteristics
- 1 : 2 demultiplexed output (TTL level)

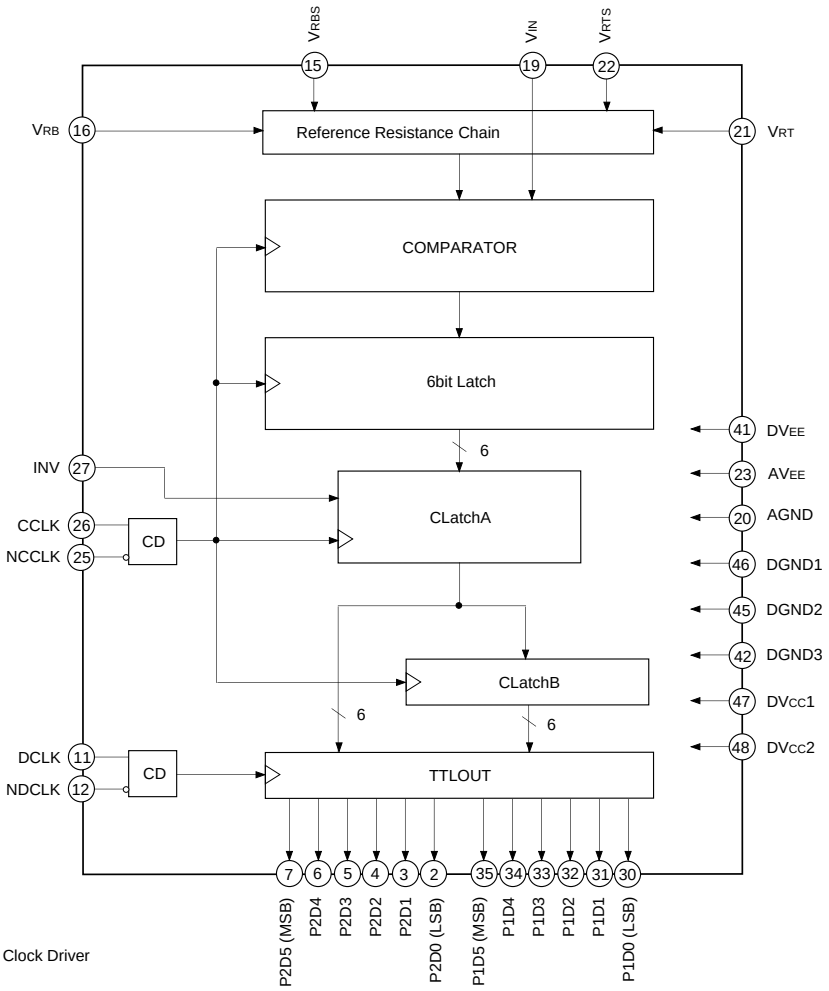
Structure

Bipolar silicon monolithic IC

Applications

- Magnetic recording (PRML)
- Communications (QPSK, QAM)
- Liquid crystal display

Block Diagram



CD; Clock Driver

E93Z35B77

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	–7.0 to +0.5	V
	DV_{CC}*1	0.5 to +7.0	V
• Analog input voltage	V_{IN}	–2.7 to +0.5	V
• Reference input voltage	V_{RT}, V_{RB}	–2.7 to +0.5	V
	I V_{RT} – V_{RB} I	2.5	V
• Digital input voltage	DIN*2	–4.0 to +0.5	V
	I CCLK – NCCLK I, I DCLK – NDCLK I	2.5	V
• Digital output current	ID0 to ID6	–30 to +30	mA
• Storage temperature	Tstg	–65 to +150	°C
• Ambient operating temperature	Ta	–20 to +75	°C
• Allowable power dissipation	P_D	750	mW

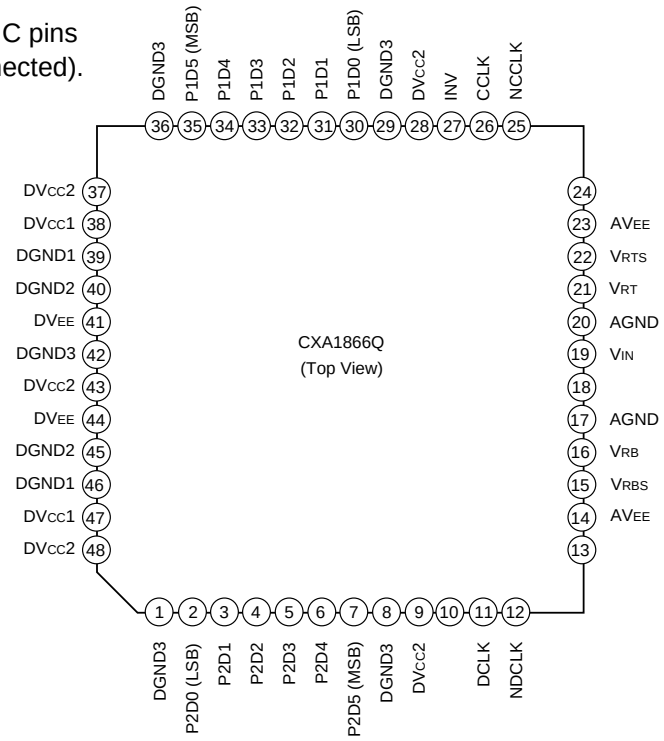
Recommended Operating Conditions

		Min.	Typ.	Max.	
• Supply voltage	AV_{EE}, DV_{EE}	–5.5	–5.2	–4.75	V
	AV_{EE} – DV_{EE}	–0.05	0	0.05	V
	AGND – DGND*3	–0.05	0	0.05	V
	DV_{CC}*1	4.75	5.0	5.25	V
• Reference input voltage	V_{RT}	–0.1	0	0.1	V
	V_{RB}	–2.2	–2.0	–0.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Digital input voltage	DIN (H)	–1.1			V
	DIN (L)			–1.5	V
• CCLK, NCCLK frequency	Fcclk			140	MHz
• DCLK, NDCLK frequency	Fdclk			70	MHz
• CCLK, NCCLK duty	Dcclk	40	50	60	%
• DCLK, NDCLK duty	Ddclk	40	50	60	%
• CCLK-DCLK time difference*4	tdcd	$–T_{PWL}$ + 2	0	T_{PWH} + 1	ns
• Operating temperature	Ta	–20		+75	°C

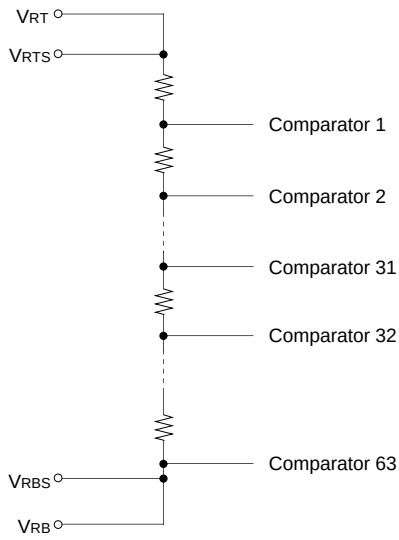
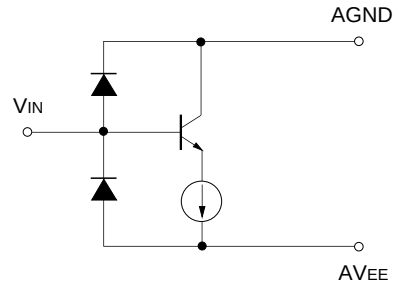
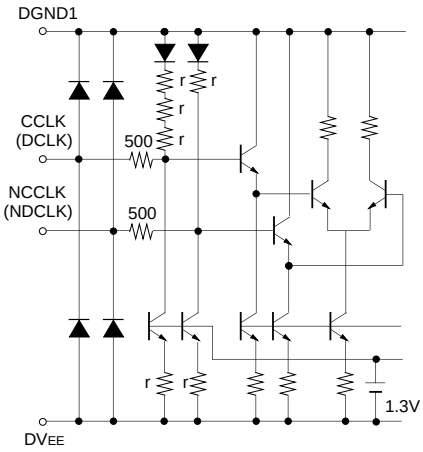
*1 DV_{CC} = DV_{CC}1, DV_{CC}2
*2 D_{IN} = CCLK, NCCLK, DCLK, NDCLK, INV
*3 DGND = DGND1, DGND2, DGND3
*4 Refer to the Timing Chart 1 for T_{PWL}, T_{PWH}.

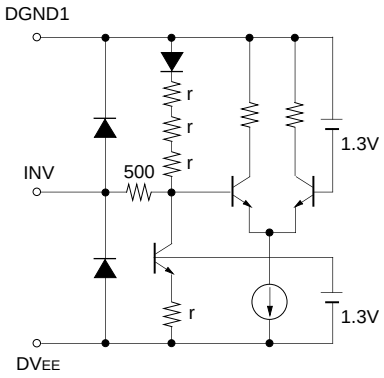
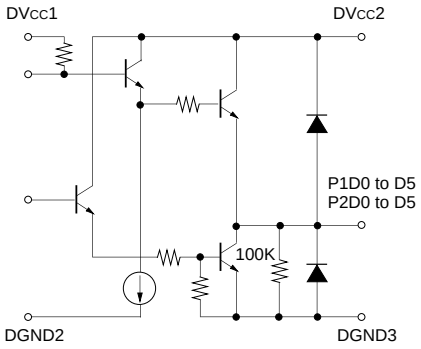
Pin Configuration.

Pins without names are NC pins (not connected).



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
21	V_{RT}	I	0V		Top reference voltage input (= 0V). This is the top reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the plus side of the input analog signal amplitude.
22	V_{RTS}	O	0V		V_{RT} sense output. This is the voltage sense pin for V_{RT}.
16	V_{RB}	I	–2V		Bottom reference voltage input (= –2V). This is the bottom reference voltage supplied to the internal resistance chain. The external input can be set in accordance with the peak value on the minus side of the input analog signal amplitude.
15	V_{RBS}	O	–2V		V_{RB} sense output. This is the voltage sense pin for V_{RB}.
19	V_{IN}	I	V_{RTS} to V_{RBS}		Analog input. The input range is 2Vp-p.
26	CCLK	I	ECL		CCLK clock input. This is the conversion clock, and is an ECL level input.
25	NCCLK	I	ECL		CCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (–1.3V). Only CCLK input can be used for operation with the NCCLK input left open,but complementary input is recommended to attain fast and stable operation.
11	DCLK	I	ECL		DCLK clock input. This is the 1:2 DMPX latch clock; input a clock of 1/2 frequency of CCLK. Data are output from DMPX port 1 and port 2 synchronously with the rising edge of this signal. This is an ECL level input.
12	NDCLK	I	ECL		DCLK inversion clock input. This is an ECL level input. When left open, this input goes to the ECL threshold potential (–1.3V). Only DCLK input can be used for operation with the NDCLK input left open, but complementary input is recommended to attain fast and stable operation.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
27	INV	I	ECL		Digital output polarity inversion input. This is an ECL level input. This input inverts the polarity of the digital outputs P1D0 to P1D5, and P2D0 to P2D5. (Refer to the Output Code Table.) When left open, this signal is maintained at the low level.
30	P1D0	O	TTL		These pins are for the 6 bits of digital output data for DMPX port 1. P2D5 is the MSB, and P2D0 is the LSB. These are TTL level outputs.
31	P1D1				
32	P1D2				
33	P1D3				
34	P1D4				
35	P1D5				
2	P2D0				These pins are for the 6 bits of digital output data for DMPX port 2. P2D5 is the MSB, and P2D0 is the LSB. These are TTL level outputs.
3	P2D1				
4	P2D2				
5	P2D3				
6	P2D4				
7	P2D5				
38, 47	DVcc1	—	+5.0V		+5V power supply for TTL level internal circuit.
9, 28, 37, 43, 48	DVcc2	—	+5.0V		+5V power supply for TTL level output buffers (P1D0 to P2D5).
39, 46	DGND1	—	0V		Ground for DVEE digital circuit.
40, 45	DGND2	—	0V		Ground for DVcc1 digital circuit.
1, 8, 29, 36, 42	DGND3	—	0V		Ground for DVcc2 digital circuit.
17, 20	AGND	—	0V		Ground for AVEE analog circuit . Used as the ground for the comparator input buffers, latches, etc. Separated from DGND.
41, 44	DVEE	—	–5.2V		–5.2V power supply for digital circuit. Connected internally with AVEE. (Resistance is 4 to 6Ω.)
14, 23	AVEE	—	–5.2V		–5.2V power supply for analog circuit. Connected internally with DVEE. (Resistance is 4 to 6Ω.)

Electrical Characteristics (Ta = 25°C, AV_{EE} = DV_{EE} = –5.2V, DV_{CC} = 5V, V_{RT} = 0V, V_{RB} = –2V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n			6		bits
DC characteristics						
Integral linearity error	EIL	Fc = 140MHz			±0.2	LSB
Differential linearity error	EDL	Fc = 140MHz			±0.2	LSB
No missing code				Guaranteed		
Analog input						
Analog input capacitance	CIN	V_{IN} = –1V + 0.07Vrms, DC ≤ V_{IN} ≤ 70MHz		7		pF
Analog input resistance	RIN	–2V ≤ V_{IN} ≤ 0V	200			kΩ
Input bias current	IIN	–2V ≤ V_{IN} ≤ 0V			110	µA
Reference input						
Reference resistance	RREF			225		Ω
Reference resistance current	Iref			9		mA
Offset voltage V_{RT}	EOT				25	mV
Offset voltage V_{RB}	EOB				25	mV
Digital input						
Logic high level	VIH		–1.13			V
Logic low level	VIL				–1.50	V
Logic high current	IIH	VIH = –0.8V	0		50	µA
Logic low current	IIL	VIL = –1.6V	–50		50	µA
Input capacitance				3.5		pF
Switching characteristics						
Maximum conversion frequency	FC	Error rate1E-9 TPS*1	140			MSPS
Aperture jitter	Taj			5.0		ps
Sampling delay	Tds			1.0		ns
Digital output						
Logic high level	VOH	IOUT = –2mA	2.7			V
Logic low level	VOL	IOUT = 1mA			0.5	V
Output delay	tdo	ZL = 25pF	2.0		8.0	ns
Output rising time	tr	ZL = 25pF, 0.5V to 2.4V		1.2		ns
Output falling time	tf	ZL = 25pF, 0.5V to 2.4V		1.2		ns
Dynamic characteristics						
Analog amplitude input bandwidth	Finb	V_{IN} = 2Vp-p, p-p value = 3dB down input frequency	210			MHz
S/N ratio	SNR1	Fc = 140MHz, Fin = 1MHz		36		dB
	SNR2	Fc = 140MHz, Fin = 35MHz		34		dB
	SNR3	Fc = 140MHz, Fin = 70MHz		32		dB
Error rate		Fc = 140MHz, error > 4LSB		10^{-9}		TPS*1
Power supply						
Supply current	ICC	DV_{CC} = +5V		20	32	mA
	IEE	AV_{EE} = DV_{EE} = –5.2V	–60	–40		mA
Power consumption	Pd			325		mW

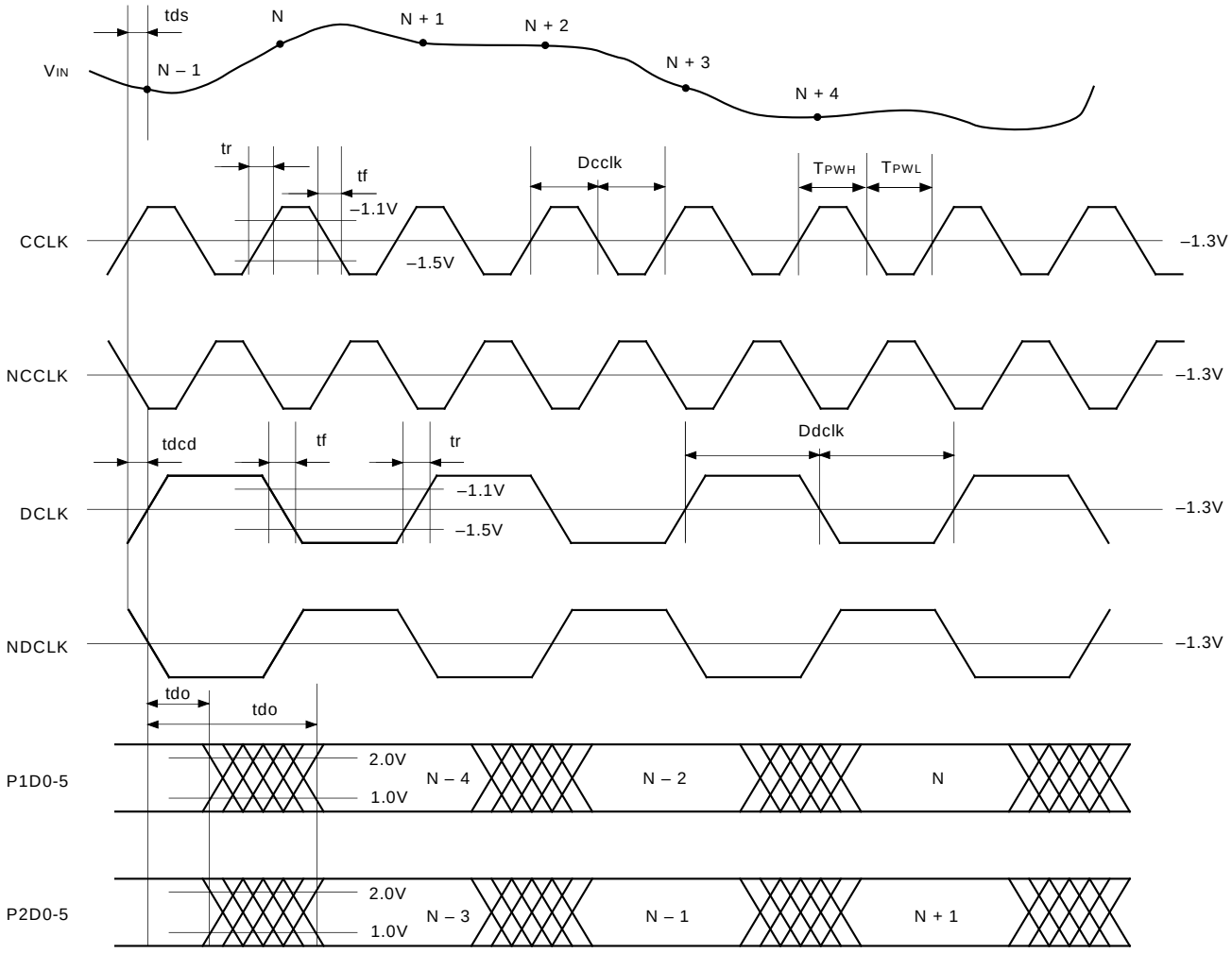
*1 TPS: Times Per Sample

Output Code Table

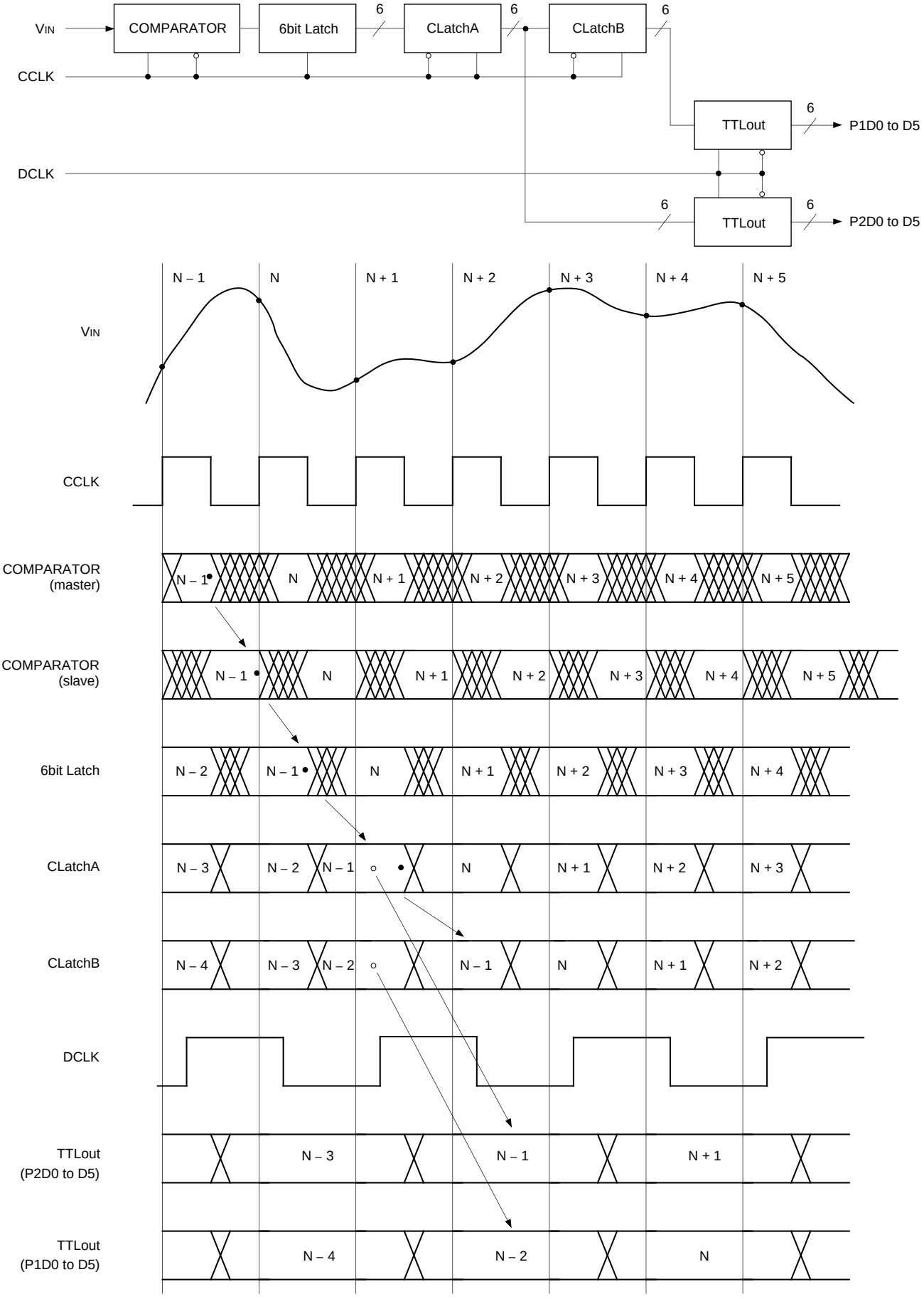
V_{IN}	STEP	INV = 0	INV = 1
		D5 D0	D5 D0
0V	0	0 0 0 0 0 0	1 1 1 1 1 1
	1	0 0 0 0 0 1	1 1 1 1 1 0
		:	:
–1V	31	0 1 1 1 1 1	1 0 0 0 0 0
	32	1 0 0 0 0 0	0 1 1 1 1 1
		:	:
		1 1 1 1 1 0	0 0 0 0 0 1
–2V	63	1 1 1 1 1 1	0 0 0 0 0 0

* INV = 0: low level; INV = 1: high level

Timing Chart 1

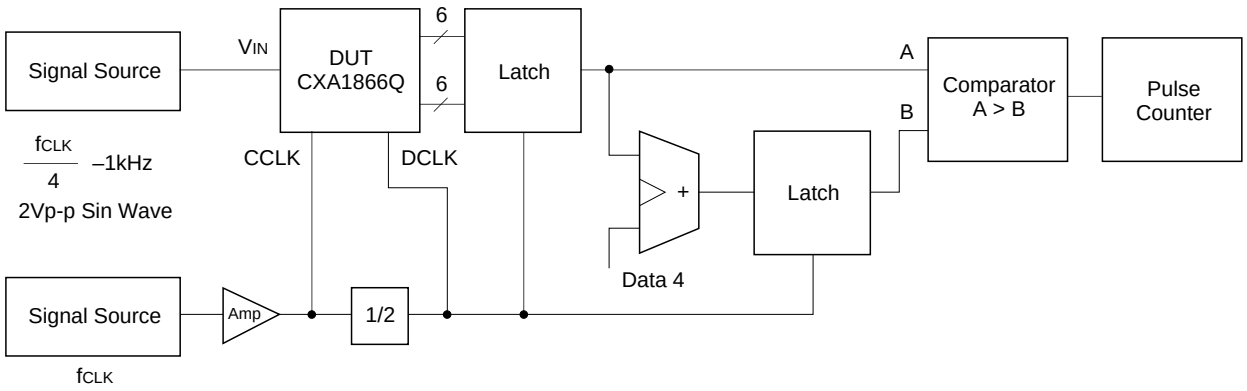


Timing Chart 2

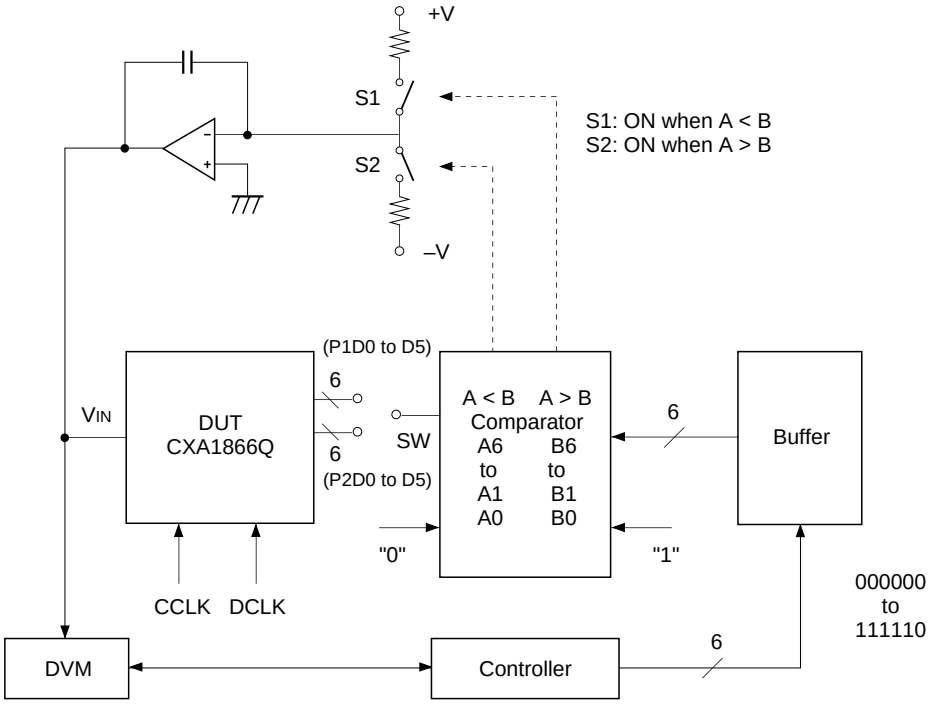


Electrical Characteristics Measurement Circuit

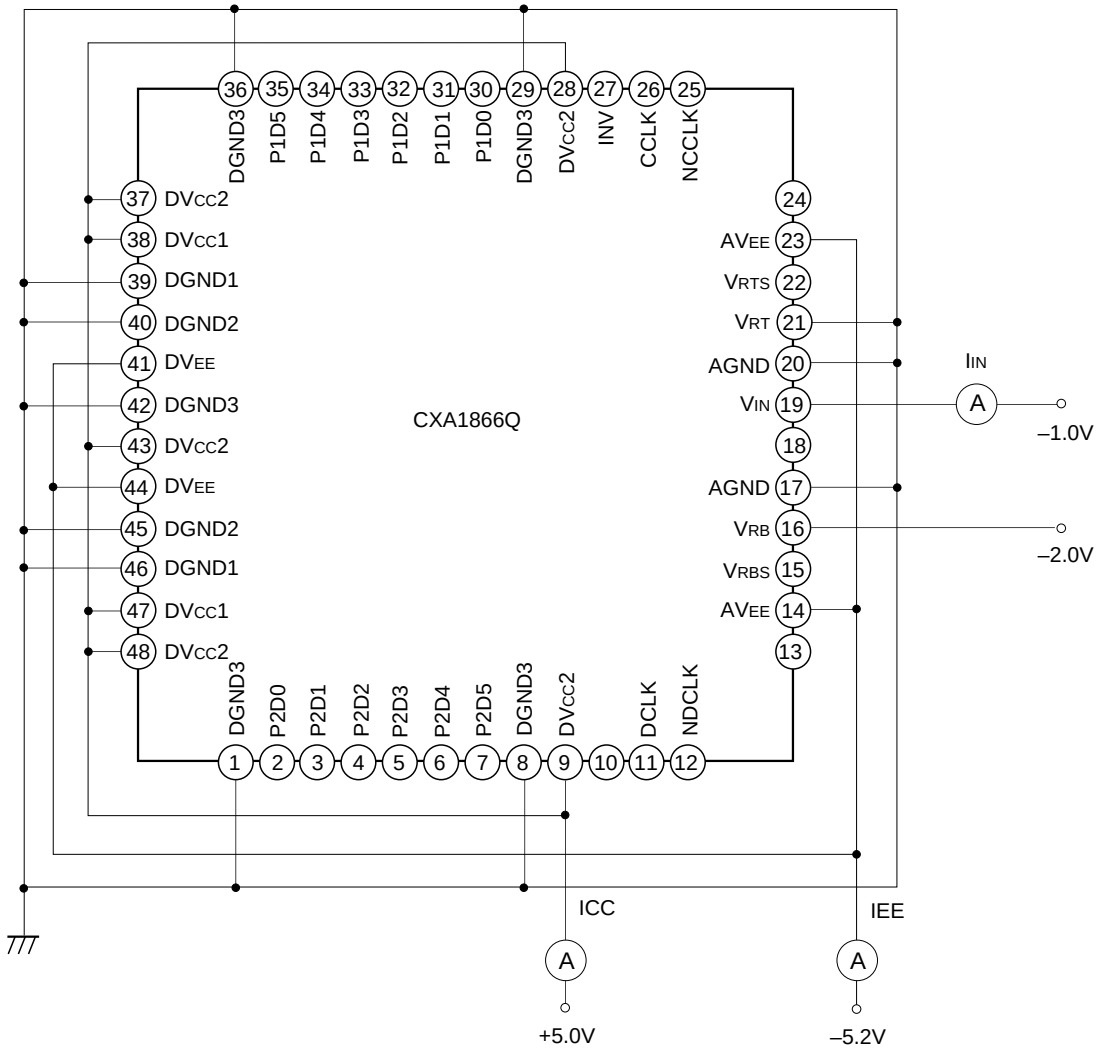
Maximum conversion rate measurement circuit



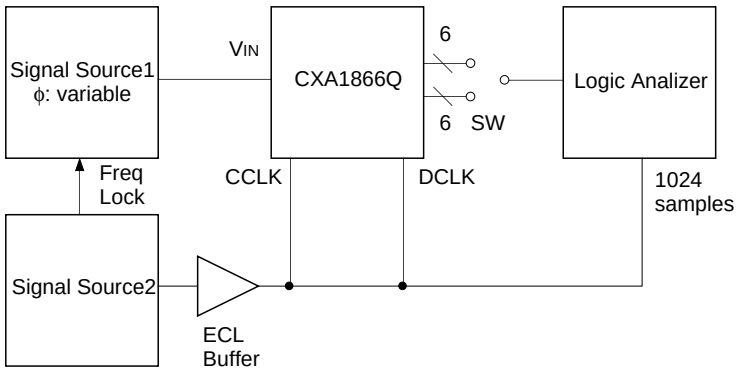
Integral linearity error measurement circuit
Differential linearity error measurement circuit



Current consumption measurement circuit
Analog input bias measurement circuit

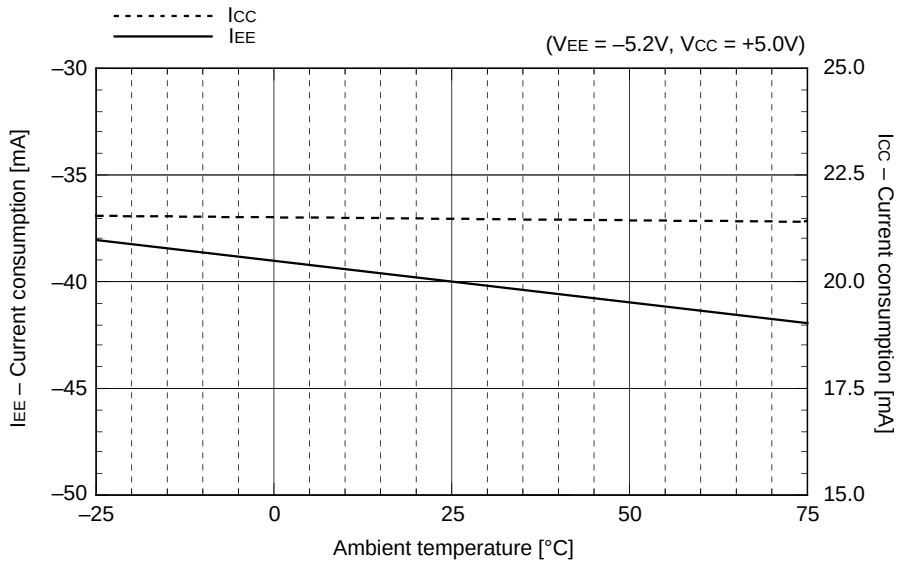


Sampling delay measurement circuit
Aperture jitter measurement circuit

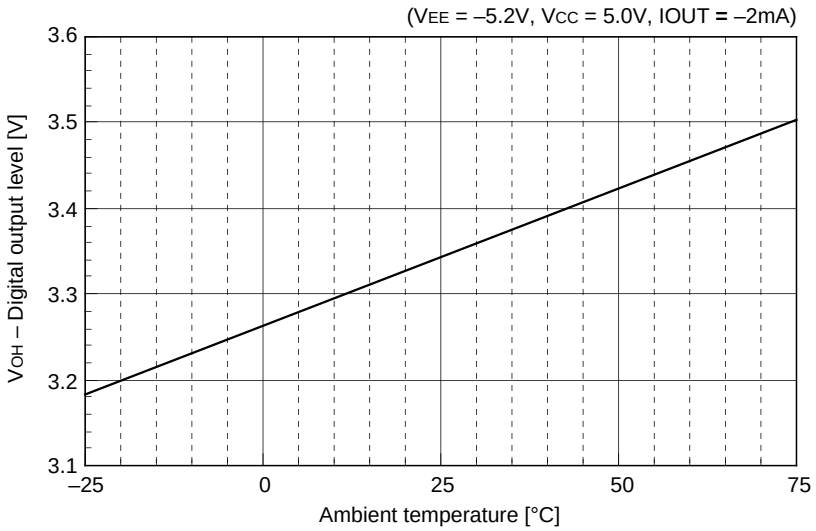


Electrical Characteristics

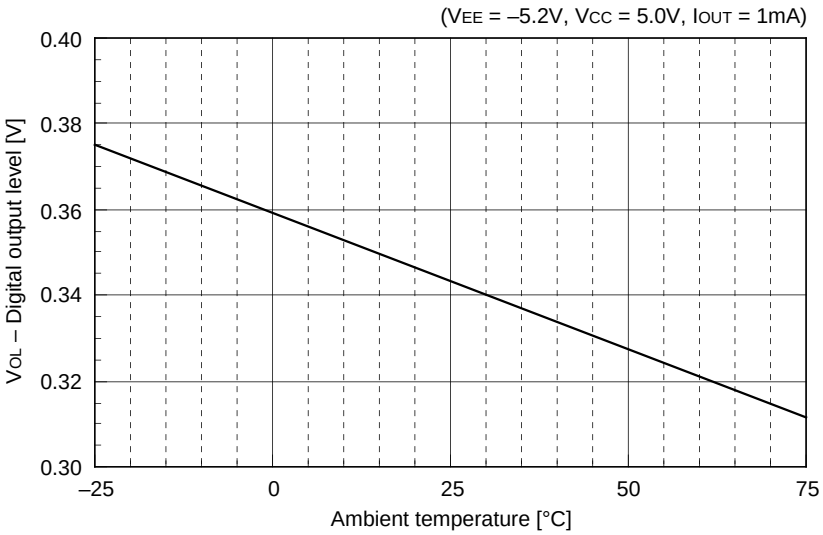
Current comsumption vs. Ambient temperature



VOH vs. Ambient temperature

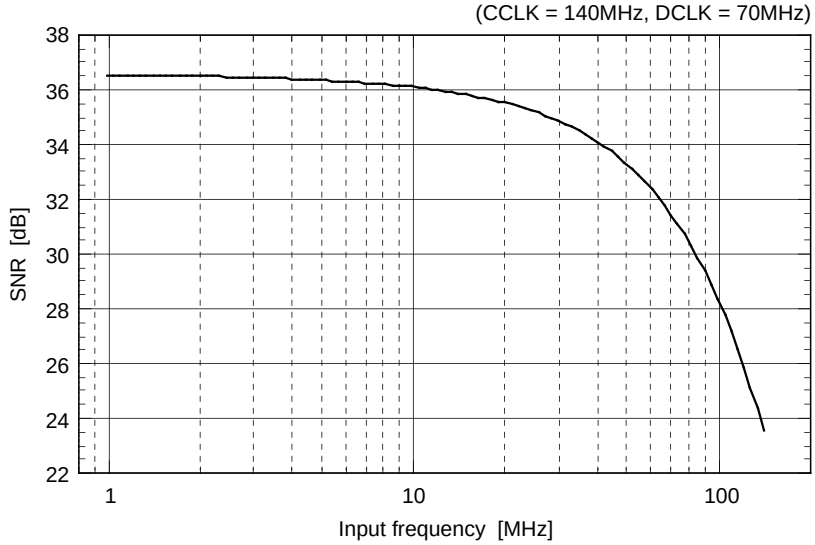


VOL vs. Ambient temperature



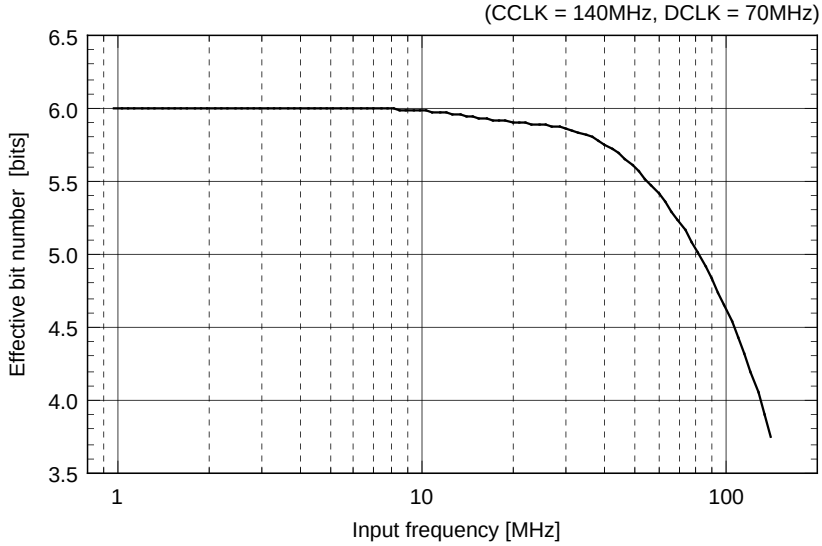
SNR vs. Input frequency

(CCLK = 140MHz, DCLK = 70MHz)



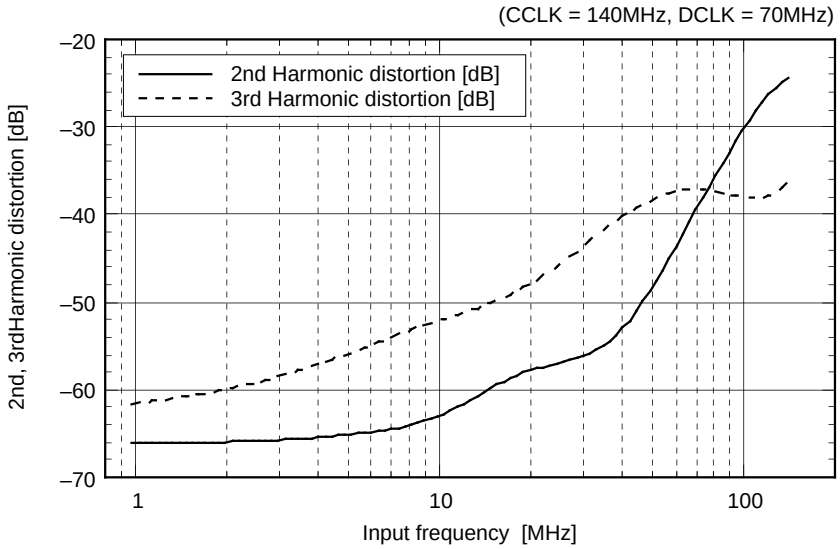
Effective bit number vs. Input frequency

(CCLK = 140MHz, DCLK = 70MHz)



2nd, 3rd Harmonic distortion vs. Input frequency

(CCLK = 140MHz, DCLK = 70MHz)



Notes on Operation

The CXA1866Q is a high speed A/D converter with ECL level logic input and demultiplexed TTL level output. Take notice of the followings to ensure optimum performance from this IC.

<<Power Supply and Grounding>>

- Grounding has a profound influence on converter performance. The higher the frequency is, the more important the way of grounding becomes.

- The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using the multi-layer board.

- To prevent interference between the AGND and DGND patterns and between the AV_{EE} and DV_{EE} lines, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{EE} and DV_{EE} lines at one point each via a ferrite-bead filter. Shorting analog and digital ground patterns in one place immediately under the A/D converter improves A/D converter performance.

- Ground the power supply pins (AV_{EE}, DV_{EE}, DVcc) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AV_{EE} pin to the AGND pattern, DV_{EE} to DGND, and DVcc to DGND.)

<<Analog Input>>

- Make the connection between the V_{IN} pin and the analog input source as short as possible.

- There is a slight offset voltage at reference voltage pins V_{RT} and V_{RB}. If it presents no problem in the application, the voltage can be applied directly. However, if the reference voltage is to be set precisely, apply it via a feedback circuit created using the V_{RTS} and V_{RBS} pins.

- Make adequate by-pass for high frequency noise at V_{RT} and V_{RB}. The V_{RT} pin is normally connected to AGND on the board. Bypass the V_{RB} pin to the AGND pattern with a 0.1µF or larger ceramic chip capacitor as short as possible. The 10µF tantalum capacitor connected to V_{RB} in the Application Circuit is to stop oscillation in the reference voltage generation circuit.

<<Digital Input>>

- Noise at the INV pin may cause misoperation of which the cause is extremely hard to identify. If it is OK for the set voltage level to be low only, leave the pin open. If a high level voltage have to be input, bypass the INV pin to DGND with an about 0.1µF ceramic chip capacitor as short as possible. It is recommend that high level input voltage is about –0.5V to –1.0V, and low level input voltage is about –1.6V to –2.5V. When inputting a high level voltage, avoid connecting directly to DGND.

- The CXA1866Q has input pins for two clocks: CCLK and DCLK. For CCLK, which is used for the internal comparator, input an ECL level clock with up to the maximum conversion frequency. For DCLK, which is used for the multiplex output, input an ECL level clock with a rate half that of CCLK. Take notice of the timing between CCLK and DCLK.

- It is recommended that differential signals be input to the clock input pins CCLK, NCCLK, DCLK and NDCLK. The A/D converter can be driven only by the clock input pins CCLK and DCLK, but there is a risk of unstable characteristics at maximum speeds.

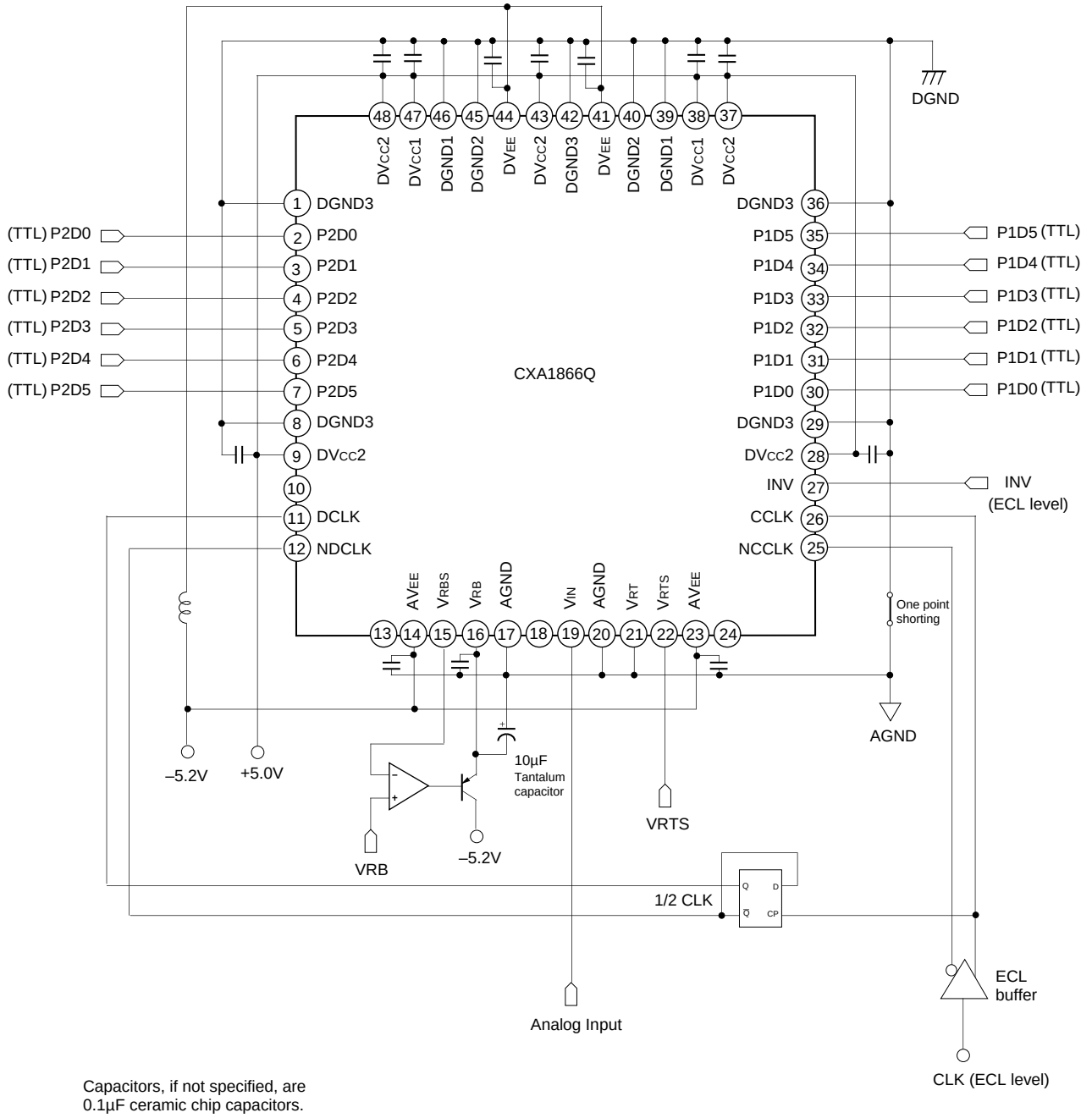
- If the NCCLK and NDCLK pins are not used, bypass these pins to DGND with an about 0.1µF capacitor. In this time, about –1.3V voltage is generated at the NCCLK and NDCLK pins. However, this is too weak to be used as threshold voltage V_{BB}; it can not directly drive even one ECL input load.

- The clock duty cycle is designed for use at 50%. Any diversion from this percentage will have a slight effect on the maximum performance of the A/D converter, but there is no great need for adjustment.

<<Digital Output>>

- P1D0 (LSB) to P1D5 (MSB), and P2D0 (LSB) to P2D5 (MSB) are demultiplex digital outputs (2 systems), and are output using the DCLK timing. The polarity of the output data can be inverted using the INV signal.

Application circuit



Capacitors, if not specified, are 0.1µF ceramic chip capacitors.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

CXA1866Q-PCB (6bit, 140MSPS, ADC Evaluation Board)

Description

The CXA1866Q PCB is a tool for customers to evaluate the performance of the CXA1866Q (6bit, 140MHz, TTL demultiplexed output, high-speed A/D converter). In addition to indispensable features such as the reference voltage generator, this tool equips.

The input voltage offset generator, clock decimator, output data latches, 10-bit high-speed DAC × 2, and 26-pin cable connector for 2-system digital output.

This evaluation board provides full performance of the CXA1826Q and it is designed to facilitate evaluation.

Features

- Resolution: 6bits
- Maximum conversion rate: 140MHz
- Supply voltage: +5.0V, –5.2V
- Conversion for clock input level: Sine wave converted to ECL level signal
- Reference voltage adjustment circuit for the A/D converter
- Built-in clock frequency decimation circuit: (1/2)

Supply Current

Item	Min.	Typ.	Max.	Unit
V_{EE} (–5.2V)		2.0	2.2	A
Vcc (+5.0V)		0.6	0.7	A

Analog Input

Item	Min.	Typ.	Max.	Unit
Input voltage (AMP. IN)	–0.5		+0.5	V
(DIR. IN)	–2.0		0	V
Input impedance		50		Ω

Clock Input

Item	Min.	Typ.	Max.	Unit
Input voltage (Peak to Peak)	0.6	1.0		Vp-p
Input impedance		50		Ω

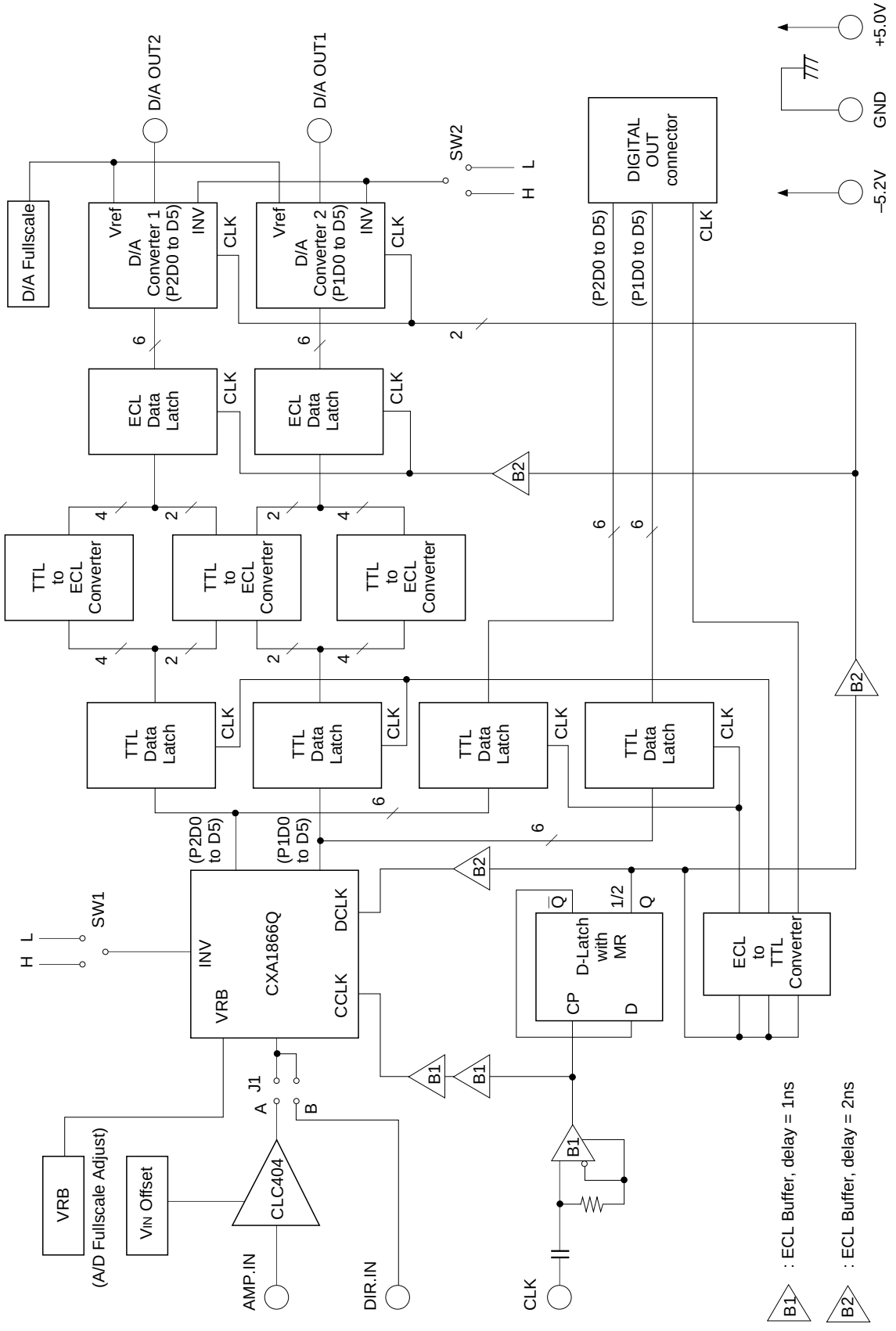
Digital Output

TTL level, demultiplexed output

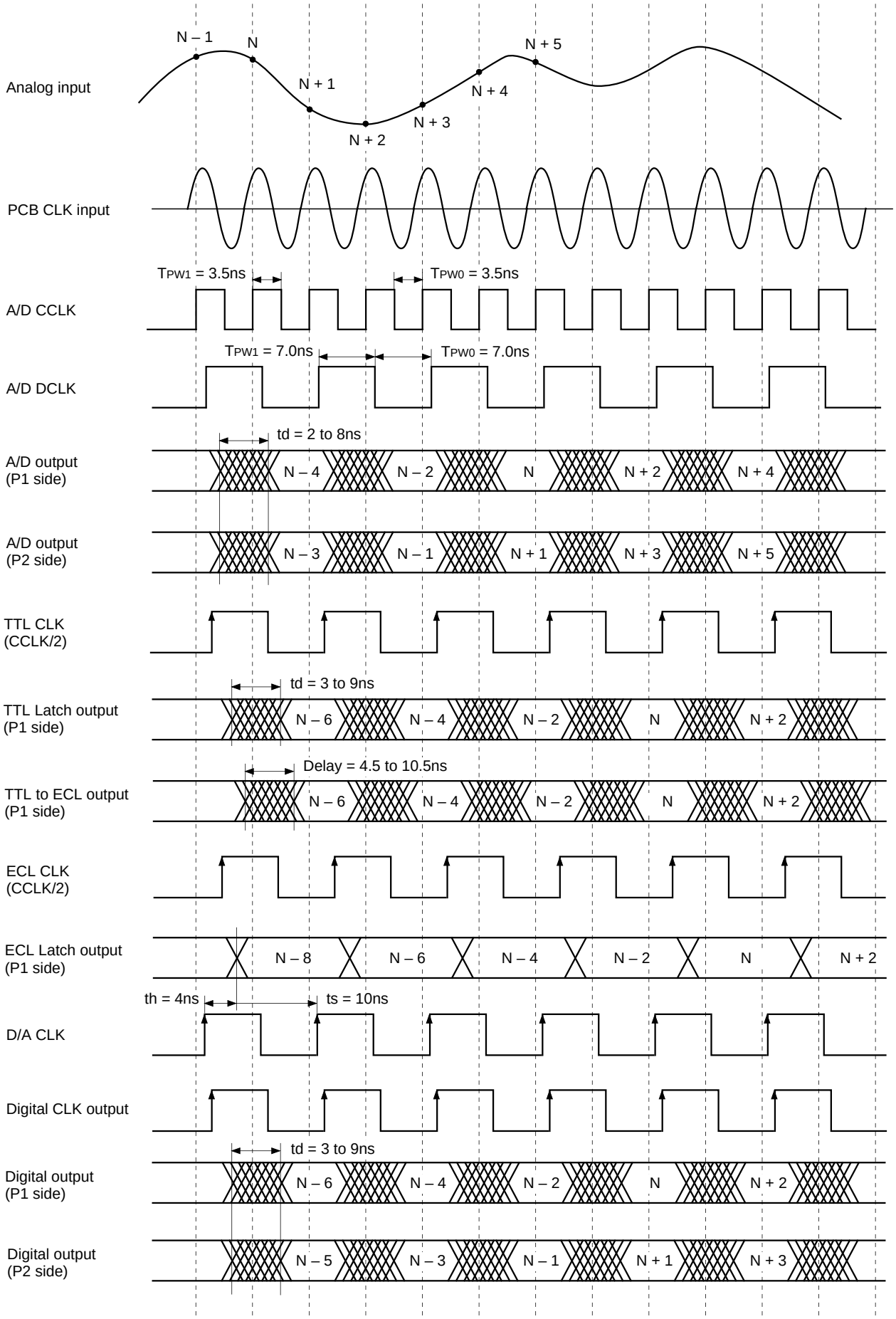
Clock Output

TTL level, Single output

Block Diagram



Timing Chart



Adjustment Methods and Notes on Operation

1) V_{IN} Offset (VR1)
   The volume to adjust the AMP. IN input signal range (0V center assumed) with the A/D converter input range.

2) A/D Full Scale (VR2)
   The volume to adjust A/D converter VRB voltage (–2V typ.).

3) D/A Full Scale (VR3)
   The volume to adjust D/A converter reference voltage (–1V typ.).

4) Input pins
   DIR. IN .....Used to directly input to A/D converter from signal generator.
   AMP. IN.....Used to input to A/D converter after amplifying the signal generator input to that of –2 times by operational amplifier.
   CLK .....Clock input for A/D converter and peripheral ICs. Input a sine wave of 1Vp-p.

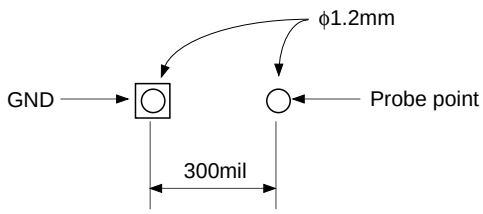
5) Output pins
   D/A OUT1 .....Analog output of D/A converter for (P1D0 to D5) data from A/D converter.
   D/A OUT2 .....Analog output of D/A converter for (P2D0 to D5) data from A/D converter.
   DIGITAL OUT .....Output of TTL CLK (1/4 decimation) and digital data (P1D0 to D5, P2D0 to D5).

6) J1 short bar is provided to use analog input pins AMP. IN and DIR. IN.

Analog input method	A	B	Offset
AMP. IN input	SHORT	OPEN	Adjust with VR1.
DIR. IN input with DC coupled	OPEN	SHORT	Input a offset signal.
DIR. IN input with AC coupled	1kΩ	0.1µF	Adjust with VR1.

7) SW1 (A/D INV), SW2 (D/A INV)
   SW1: Output inversion (INV) switch of the CXA1866Q A/D converter
   SW2: Output inversion (INV) switch of the CX20201 D/A converter

8) Waveform probe pins P5, P6, P7, P9 and P11 through P38 are devised to facilitate GND connection in order to reduce the distortion. As shown in the diagram below, the distance between the probe point and the GND is 300 mils, and there is ϕ1.2mm throughhole at each. The signal and GND locations are suit for a Tektronix GND tip (part number 013-1185-00).



Digital Out Connector Pin Assignment

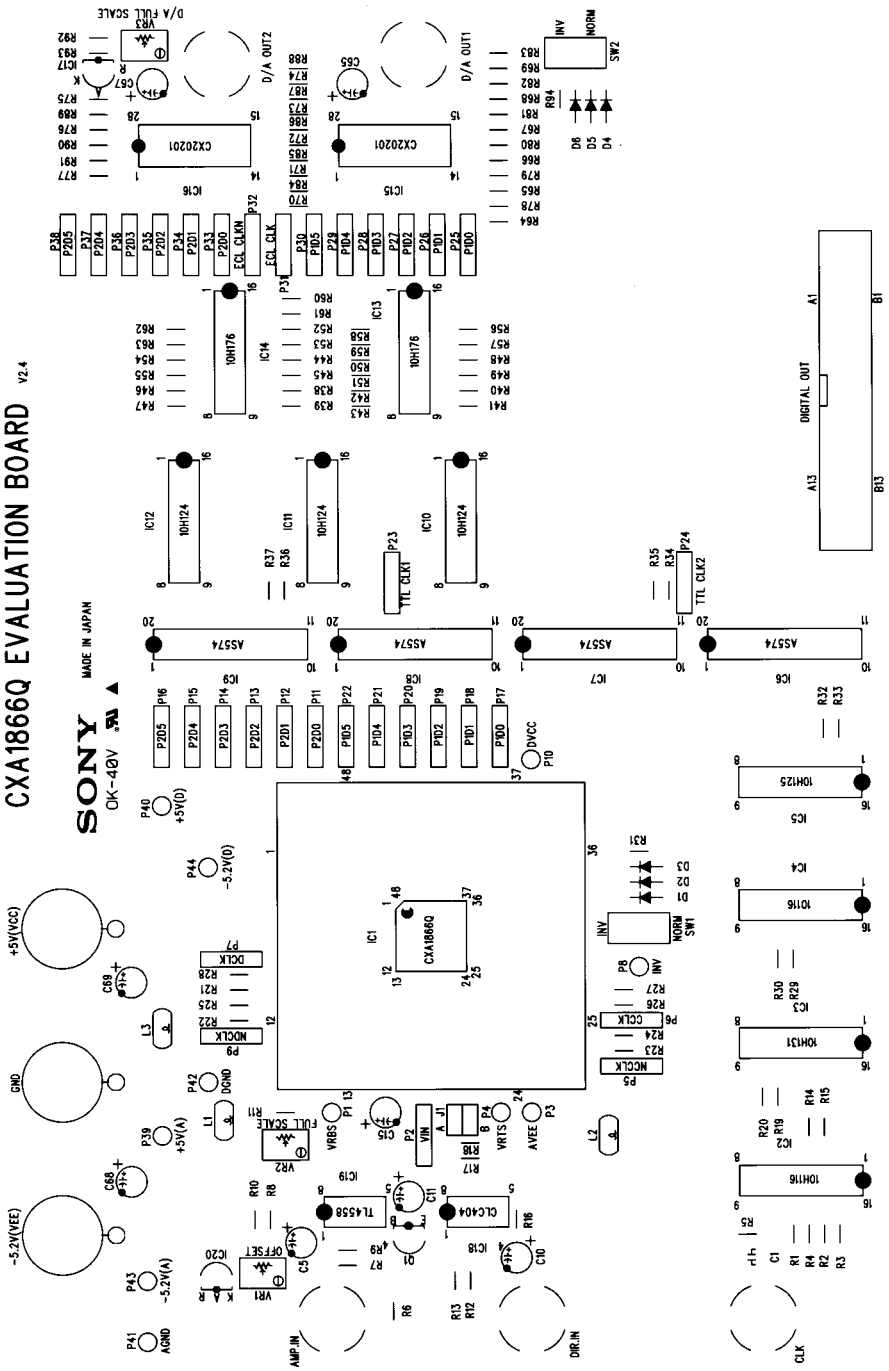
Pin No.	Assignment	Pin No.	Assignment
A1	P2D0	B1	GND
A2	P2D1	B2	GND
A3	P2D2	B3	GND
A4	P2D3	B4	GND
A5	P2D4	B5	GND
A6	P2D5	B6	GND
A7	P1D0	B7	GND
A8	P1D1	B8	GND
A9	P1D2	B9	GND
A10	P1D3	B10	GND
A11	P1D4	B11	GND
A12	P1D5	B12	GND
A13	CLK	B13	GND

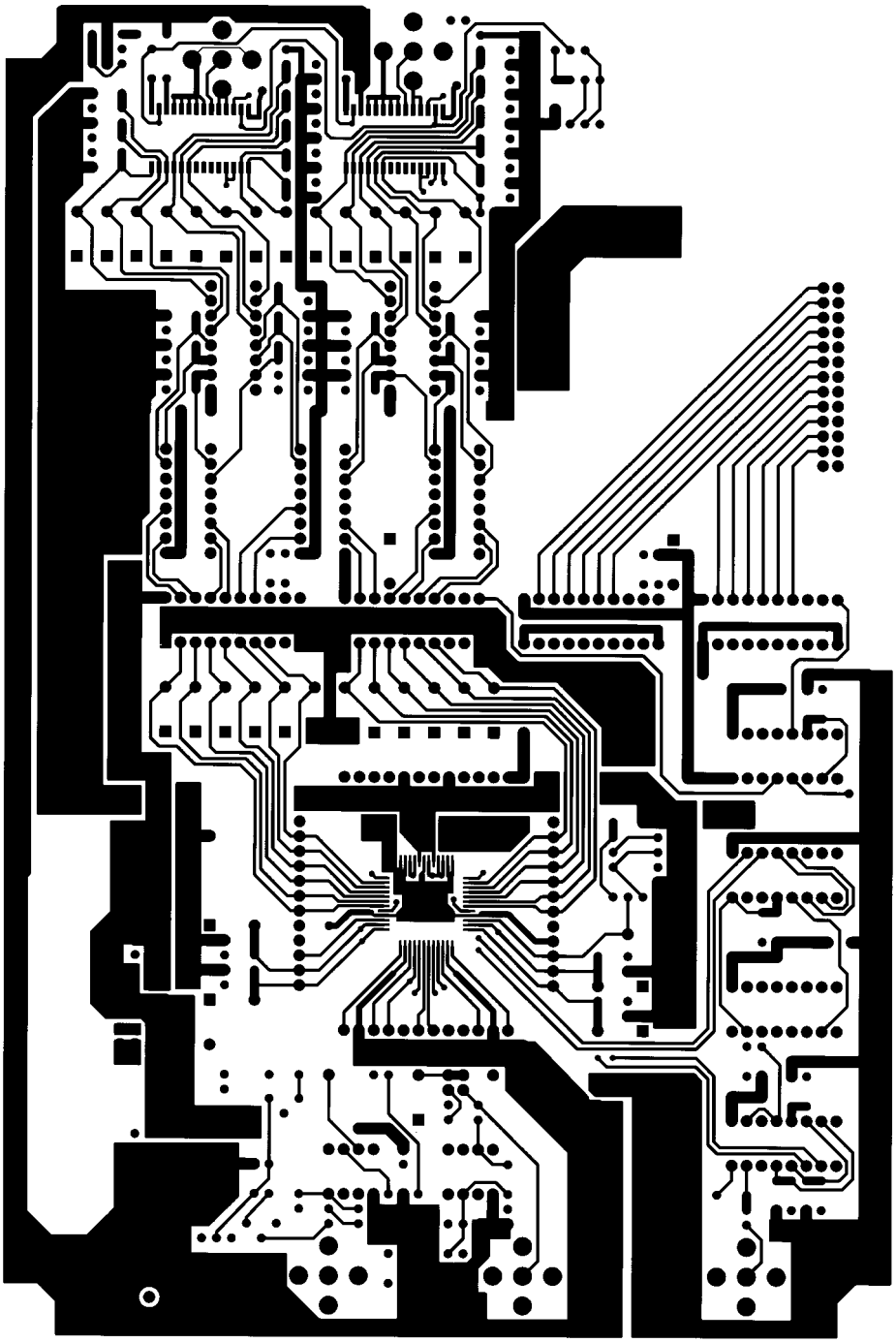
Part list

RESISTOR:	
R5, R6, R17, R18	51Ω
R3, 4, 15, 20, 21, 22, 24, 27	82Ω
R30, 33, 39, 41, 43, 45, 47	82Ω
R49, 51, 53, 55, 57, 59, 61	82Ω
R63, R78 to R91	82Ω
R1, 2, 14, 19, 23, 25, 26, 28	130Ω
R29, 32, 38, 40, 42, 44, 46	130Ω
R48, 50, 52, 54, 56, 58, 60	130Ω
R62, R64 to R77	130Ω
R10, R12	240Ω
R34 to R37, R93	270Ω
R31, R94	330Ω
R8	510Ω
R16	560Ω
R13, R92	1kΩ
R11	1.3kΩ
R7	11kΩ
R9	22kΩ
VARIABLE RESISTOR:	
VR1, 2, 3	2kΩ (RJ-5W202)
CAPACITOR:	
C1	0.1µF (CERAMIC)
C5, C65, C67	3.3µF (TANTALUM)
C11, C12, C15	1µF (TANTALUM)
C68, C69	33µF (TANTALUM)
OTHER	0.1µF (CHIP CAPACITOR)

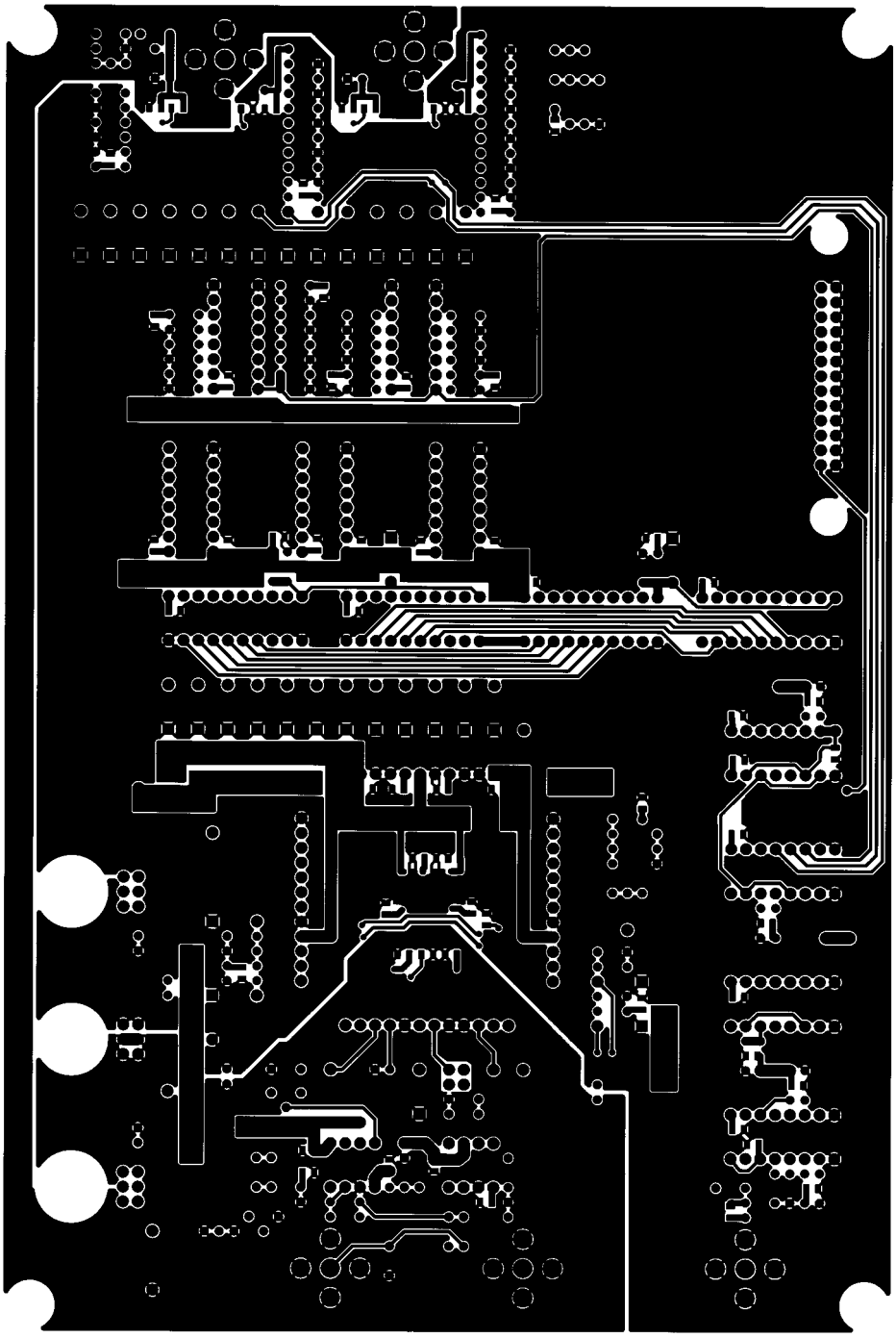
TRANSISTOR:	
Q1	2SA970
IC:	
IC2	10H116
IC3	10H131
IC4	10116
IC5	10H125
IC6 to 9	74AS574
IC10, 11, 12	10H124
IC13, 14	10H176
IC15, 16	CX20201A
IC17, IC20	TL431CLP
IC18	CLC404AJP
IC19	TL4558P
DIODE:	
D1 to D6	1S2076A
FERRITE BEAD:	
L1, L2, L3	ZBF253D-00
SWITCH:	
SW1, SW2	AT1D-2M3-10
OTHERS:	
BNC CONNECTOR	BNC-R-PC
DIGITAL OUT CONNECTOR	HIF3FB-26PA-2.54DS
JUMPER LINE	JX-1

Part Layout


CXA1866Q EVALUATION BOARD V2.4
SONY
CK-40V
MADE IN JAPAN
IC1
CXA1866Q
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16
IC18
IC19
IC20
CX20201
10H176
10H124
AS574
10H125
10H116
10H131
TL4558
CLC404
D/A OUT1
D/A OUT2
D/A FULL SCALE
DIGITAL OUT
TTL CLK1
TTL CLK2
ECL CLKN
OFFSET
FULL SCALE
INV
NORM
SW1
SW2
DCLK
NDCLK
CCLK
NCCLK
+5V(VCC)
-5.2V(VEE)
GND
+5V(D)
-5.2V(D)
DGND
+5V(A)
-5.2V(A)
AGND
DVCC
AVEE
VRBS
VRTS
AMP.IN
DIR.IN
CLK

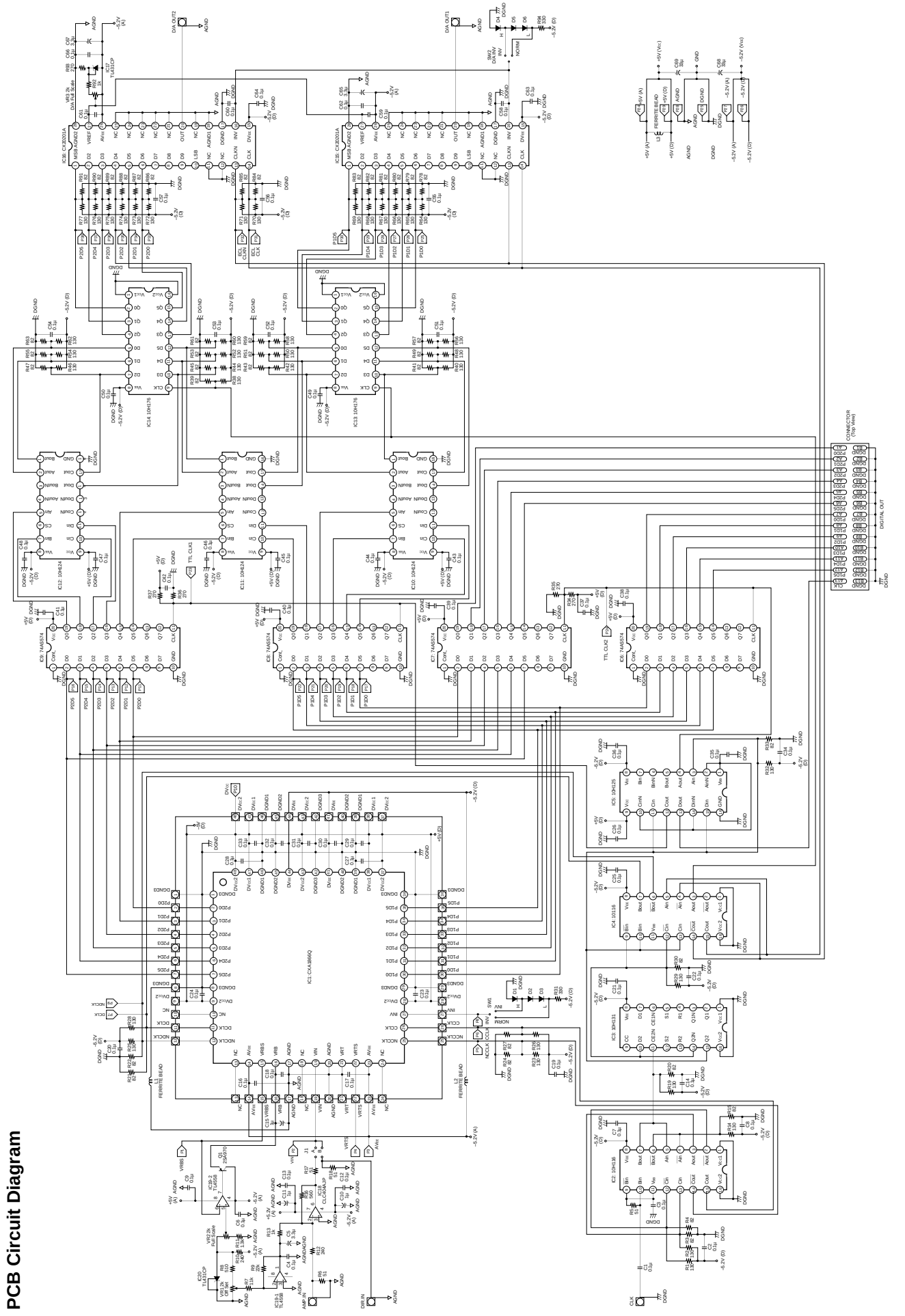


Ptinted Pattern (Component plane)



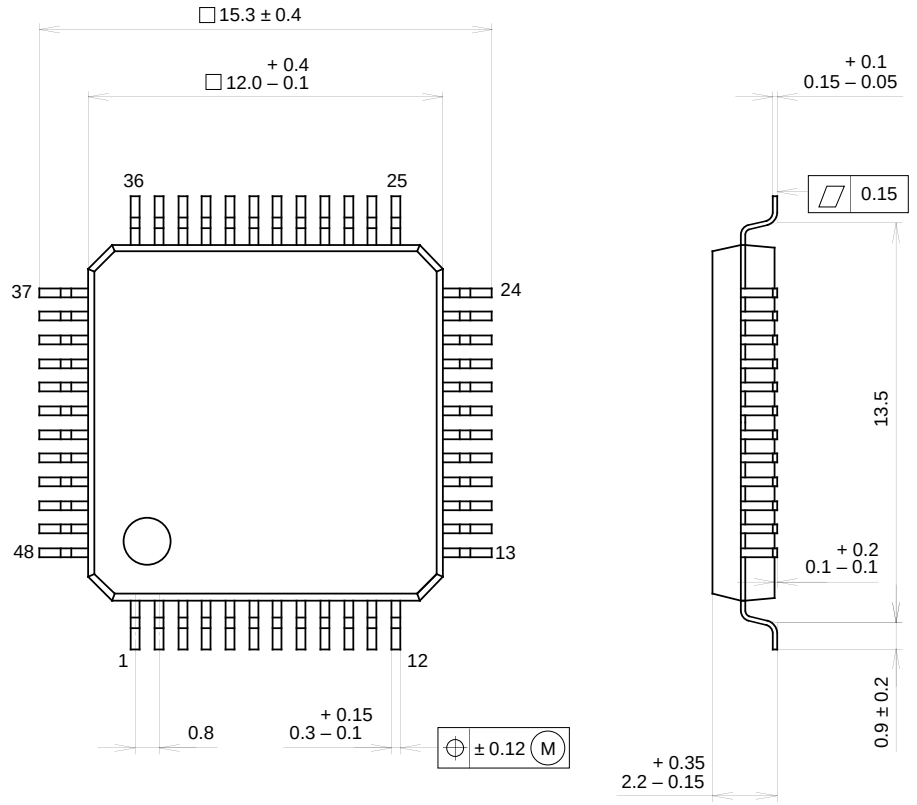
Ptinted Pattern (Solder plane)

PCB Circuit Diagram



Package Outline Unit: mm

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).