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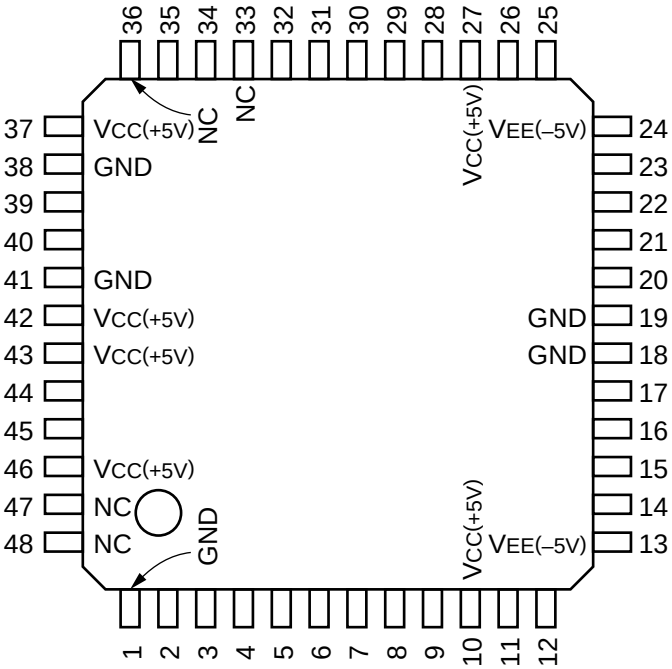
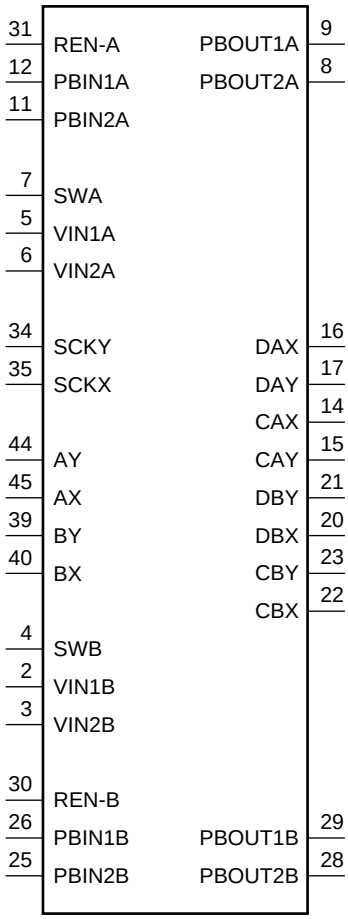
DUAL REC EQUALIZER WITH REC DRIVER

-TOP VIEW-





(VCC = +5V)
(VEE = –5V)

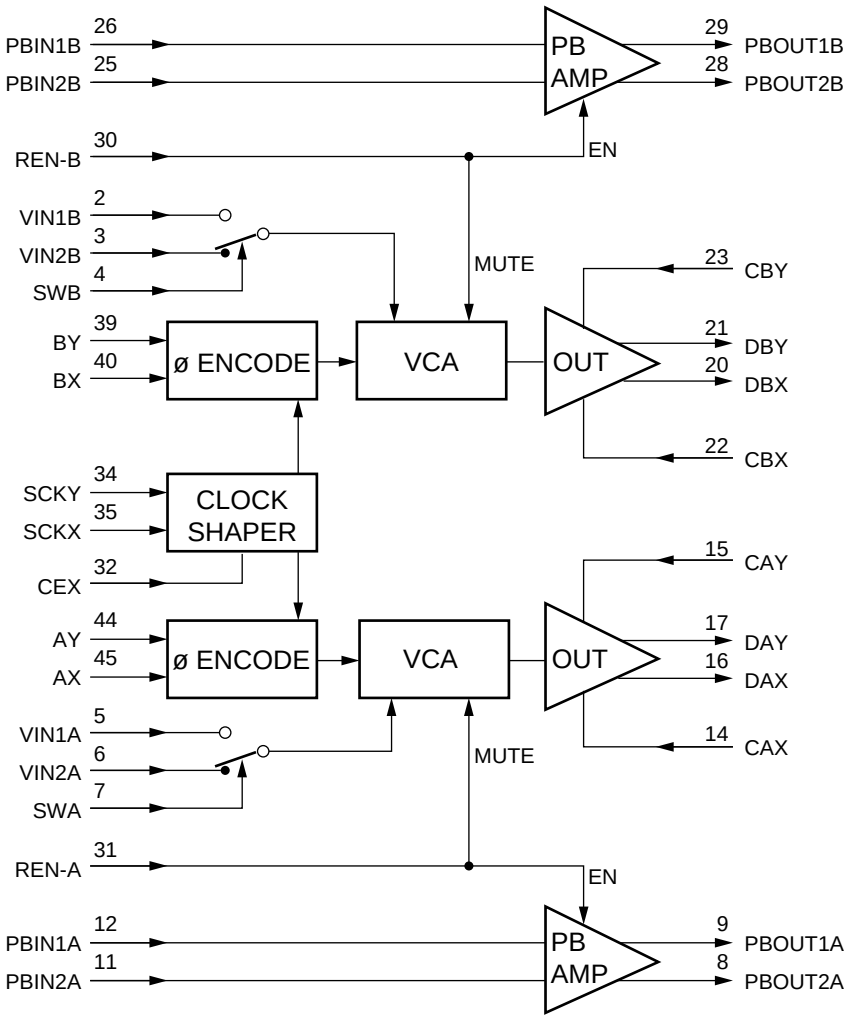
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	13	—	VEE	25	I	PBIN2B	37	—	VCC
2	I	VIN1B	14	I	CAX	26	I	PBIN1B	38	—	GND
3	I	VIN2B	15	I	CAY	27	—	VCC	39	I	BY
4	I	SWB	16	O	DAX	28	O	PBOUT2B	40	I	BX
5	I	VIN1A	17	O	DAY	29	O	PBOUT1B	41	—	GND
6	I	VIN2A	18	—	GND	30	I	REN-B	42	—	VCC
7	I	SWA	19	—	GND	31	I	REN-A	43	—	VCC
8	O	PBOUT2A	20	O	DBX	32	I	CEX	44	I	AY
9	O	PBOUT1A	21	O	DBY	33	—	NC	45	I	AX
10	—	VCC	22	I	CBX	34	I	SCKY	46	—	VCC
11	I	PBIN2A	23	I	CBY	35	I	SCKX	47	—	NC
12	I	PBIN1A	24	—	VEE	36	—	NC	48	—	NC

INPUT

AX, AY	;	REC DATA OF CHANNEL A, C
BX, BY	;	REC DATA OF CHANNEL B, D
CAX, CAY	;	FREQUENCY CHARACTERISTIC GAIN COMPENSATION OF CHANNEL A, C
CBX, CBY	;	FREQUENCY CHARACTERISTIC GAIN COMPENSATION OF CHANNEL B, D
CEX	;	CONNECTED TO DUTY COMPENSATION CAPACITOR
PBIN1A	;	PLAYBACK SIGNAL OF CHANNEL C REC HEAD
PBIN2A	;	PLAYBACK SIGNAL OF CHANNEL A REC HEAD
PBIN1B	;	PLAYBACK SIGNAL OF CHANNEL D REC HEAD
PBIN2B	;	PLAYBACK SIGNAL OF CHANNEL B REC HEAD
REN-A	;	REC ENAMLE OF CHANNELS A, C
REN-B	;	REC ENAMLE OF CHANNELS B, D
SCKX, SCKY	;	CLOCK
SWA	;	SWITCHING PULSE OF CHANNELS A, C
SWB	;	SWITCHING PULSE OF CHANNELS B, D
VIN1A	;	REC CURRENT CONTROL OF CHANNEL C
VIN2A	;	REC CURRENT CONTROL OF CHANNEL A
VIN1B	;	REC CURRENT CONTROL OF CHANNEL D
VIN2B	;	REC CURRENT CONTROL OF CHANNEL B

OUTPUT

DAX, DAY	;	REC DATA OF CHANNEL A, C
DBX, DBY	;	REC DATA OF CHANNEL B, D
PBOUT1A	;	PLAYBACK SIGNAL OF CHANNEL C REC HEAD
PBOUT2A	;	PLAYBACK SIGNAL OF CHANNEL A REC HEAD
PBOUT1B	;	PLAYBACK SIGNAL OF CHANNEL D REC HEAD
PBOUT2B	;	PLAYBACK SIGNAL OF CHANNEL B REC HEAD


PBIN1B
26
PBIN2B
25
PB
AMP
29
PBOUT1B
28
PBOUT2B
REN-B
30
EN
VIN1B
2
VIN2B
3
SWB
4
MUTE
23
CBY
BY
39
BX
40
ø ENCODE
VCA
OUT
21
DBY
20
DBX
22
CBX
SCKY
34
SCKX
35
CLOCK
SHAPER
CEX
32
15
CAY
AY
44
AX
45
ø ENCODE
VCA
OUT
17
DAY
16
DAX
14
CAX
VIN1A
5
VIN2A
6
SWA
7
MUTE
REN-A
31
EN
PBIN1A
12
PBIN2A
11
PB
AMP
9
PBOUT1A
8
PBOUT2A