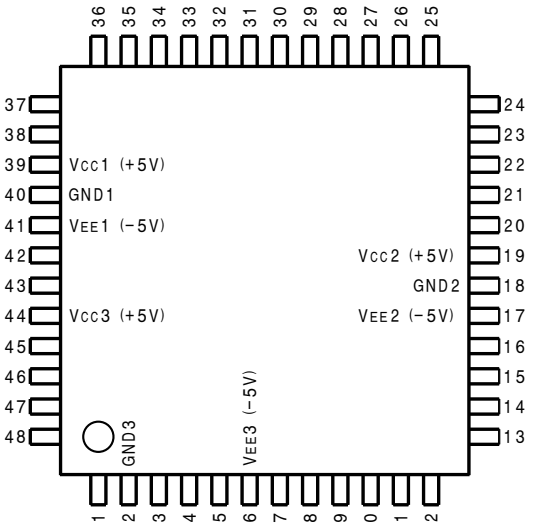
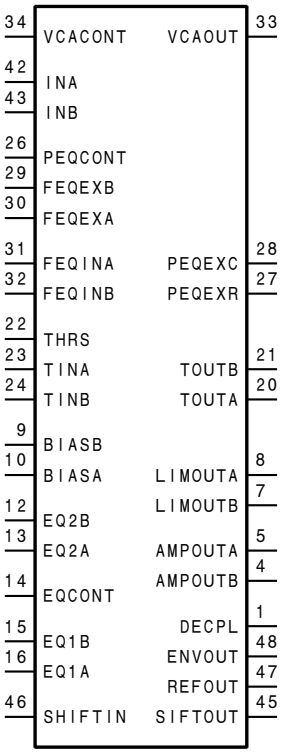
****

PB EQUALIZER

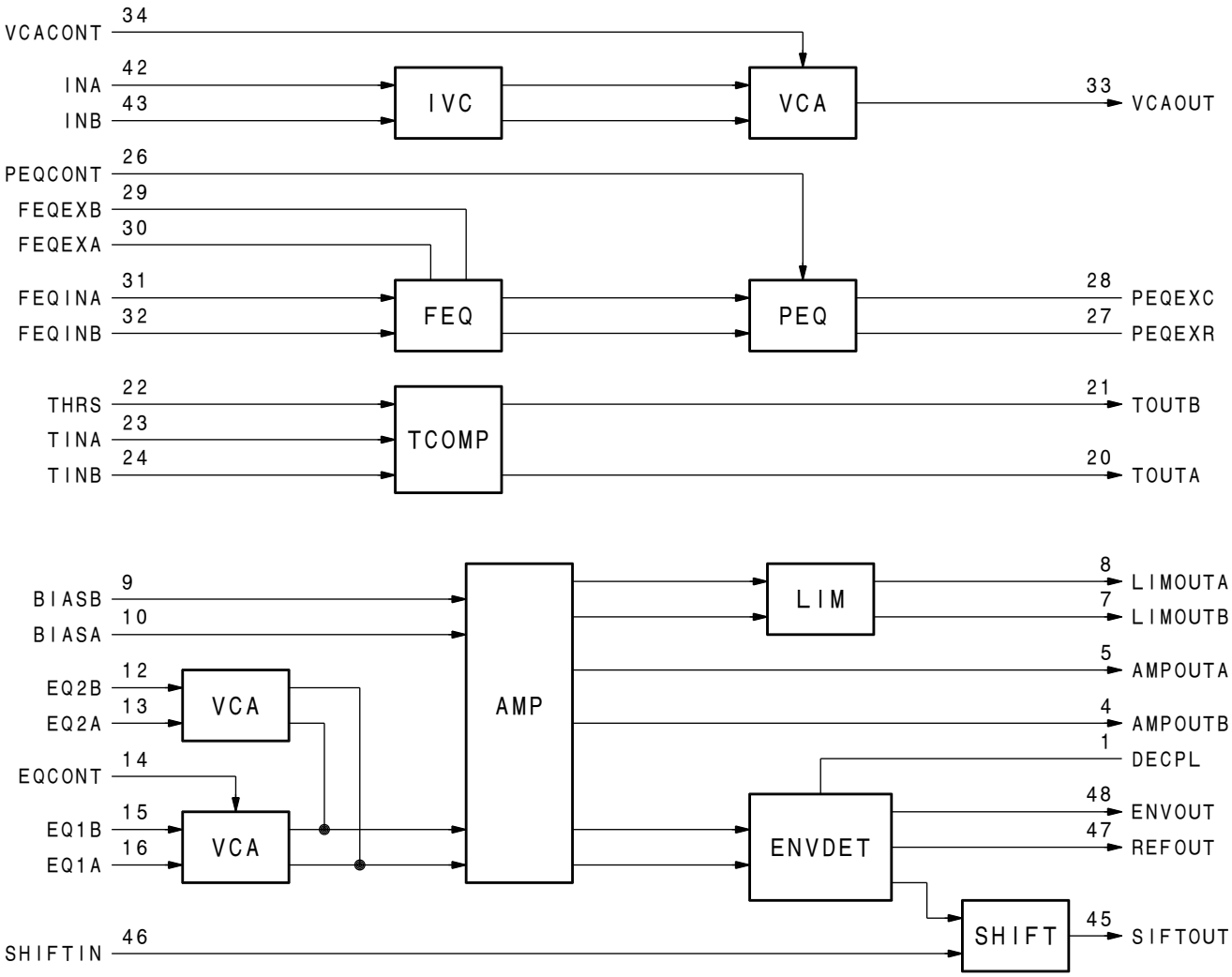
-TOP VIEW-





(VCC =+5V)
(VEE =−5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	−	DECPL	17	−	VEE2	33	O	VCAOUT
2	−	GND3	18	−	GND2	34	I	VCACONT
3	−	NC	19	−	VCC2	35	−	NC
4	O	AMPOUTB	20	O	TOUTA	36	−	NC
5	O	AMPOUTA	21	O	TOUTB	37	−	NC
6	−	VEE3	22	I	THRS	38	−	NC
7	O	LIMOUTB	23	I	TINA	39	−	VCC1
8	O	LIMOUTA	24	I	TINB	40	−	GND1
9	I	BIASB	25	−	NC	41	−	VEE1
10	I	BIASA	26	I	PEQCONT	42	I	INA
11	−	NC	27	−	PEQEXR	43	I	INB
12	I	EQ2B	28	−	PEQEXC	44	−	VCC3
13	I	EQ2A	29	−	FEQEXB	45	O	SIFTOUT
14	I	EQCONT	30	−	FEQEXA	46	I	SHIFTIN
15	I	EQ1B	31	I	FEQINA	47	O	REFOUT
16	I	EQ1A	32	I	FEQINB	48	O	ENVOUT

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INPUT
 BIASA, B       ;EQUIVALENT RF SIGNAL INPUT
 EQ2A, B        ;COSINE DELAYED SIGNAL INPUT
 EQCONT         ;COSINE CORRECTION CONTROL SIGNAL INPUT
 EQ1A, B        ;COSINE DELAYED SIGNAL INPUT
 FEQEXA, B      ;CONNECT FOR INTEGRATE CONSTANT
 FEQINA, B      ;INTEGRATOR SIGNAL INPUT
 INA            ;PLAYBACK RF SIGNAL INPUT OF CHANNEL A
 INB            ;PLAYBACK RF SIGNAL INPUT OF CHANNEL B
 PEQCONT        ;PHASE CORRECTION CONTROL SIGNAL
 SHIFTIN        ;SHIFT CIRCUIT DC SIGNAL INPUT
 TINA, B, THRS  ;THREE PRICE DETECTION CIRCUIT
 VCACONT        ;GAIN CONTROL SIGNAL

OUTPUT
 AMPOUTA, B     ;EQUIVALENT RF SIGNAL OUTPUT
 ENVOUT         ;ENVELOPE DETECTION SIGNAL
 DECPL          ;CONNECT DECOUPLING CAPACITOR FOR ENVELOPE DETECT CIRCUIT
 PEQEXC         ;CONNECT CAPACITOR FOR PHASE CORRECT
 PEQEXR         ;CONNECT RESISTOR FOR PHASE CORRECT
 REFOUT         ;ENVELOPE DETECTION SIGNAL REFERENCE
 SIFTOUT        ;NOT OFFSET ENVELOPE DETECTION SIGNAL
 TOUTA, B       ;THREE PRICE DETECTION SIGNAL
 VCAOUT         ;GAIN CONTROL SIGNAL
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