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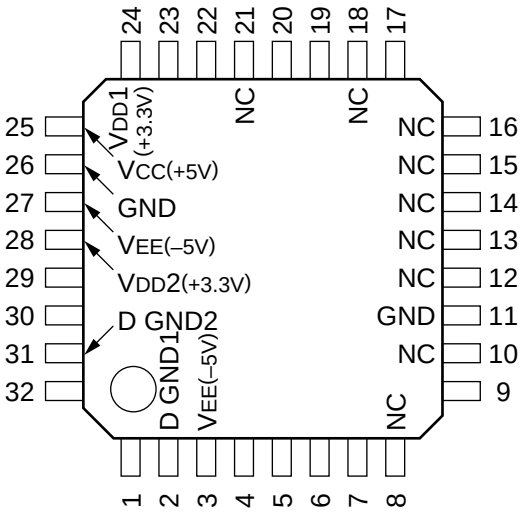
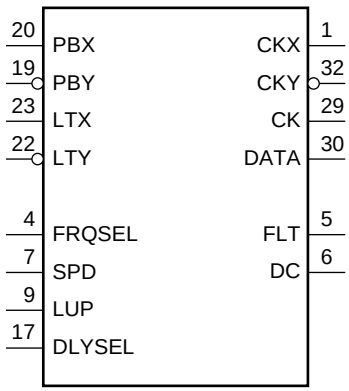
PHASE LOCKED LOOP CIRCUIT

-TOP VIEW-





PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	CKX	17	I	DLYSEL
2	—	D GND1	18	—	NC
3	—	V_{EE}	19	I	$\overline{PBY}$
4	I	FRQSEL	20	I	PBX
5	—	FLT	21	—	NC
6	—	DC	22	I	$\overline{LTY}$
7	I	SPD	23	I	LTX
8	—	NC	24	—	$V_{DD}1$
9	I	LUP	25	—	V_{CC}
10	—	NC	26	—	GND
11	—	GND	27	—	V_{EE}
12	—	NC	28	—	$V_{DD}2$
13	—	NC	29	O	CK
14	—	NC	30	O	DATA
15	—	NC	31	—	D GND2
16	—	NC	32	O	$\overline{CKY}$

INPUT

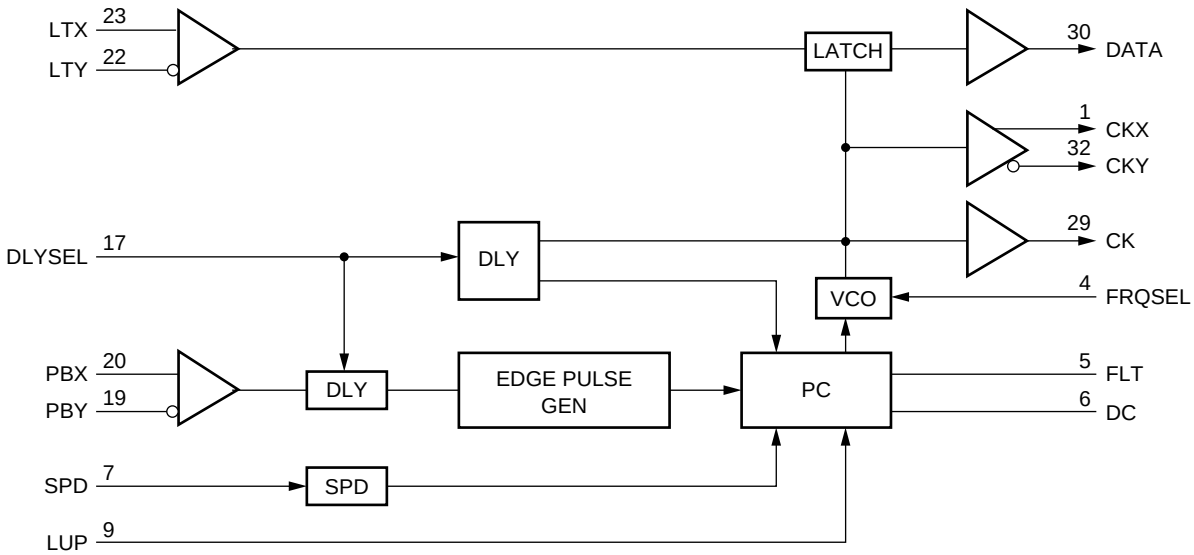
DLYSEL ; EDGE PULSE WIDTH SELECT
(H ≒ 2.5 ns, L ≒ 5 ns)
FRQSEL ; VCO OSCILLATION FREQUENCY SELECT
LTX ; LATCH INPUT (+)
LTY ; LATCH INPUT (–)
LUP ; PLL PULL-IN TIME CHANGE
PBX ; PLL INPUT (+)
PBY ; PLL INPUT (–)
SPD ; DETERMINATION OF FREE RUN FREQUENCY

OUTPUT

CK ; CLOCK OUTPUT
CKX ; CLOCK OUTPUT (+)
CKY ; CLOCK OUTPUT (–)
DATA ; DATA OUTPUT

OTHER

DC ; CONNECT DECOUPLING FOR BIAS CIRCUIT
FLT ; CONNECT CONSTANT OF LOOP FILTER


LTX
23
LTY
22
LATCH
30
DATA
1
CKX
32
CKY
29
CK
DLYSEL
17
DLY
VCO
4
FRQSEL
PBX
20
PBY
19
DLY
EDGE PULSE
GEN
PC
5
FLT
6
DC
SPD
7
SPD
LUP
9